

Regarding the usage of our schematics and alike documentation for Trenz module AM0010.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. AM0010 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

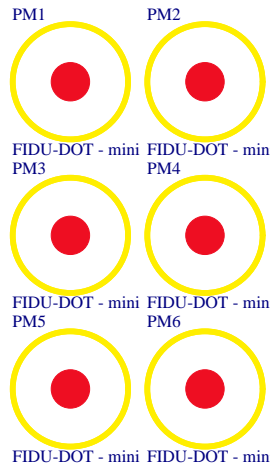
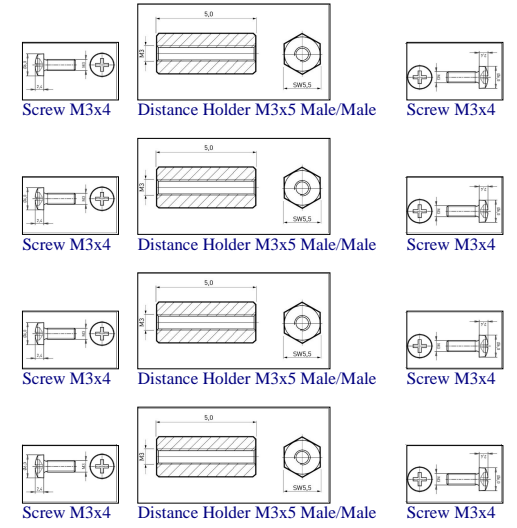
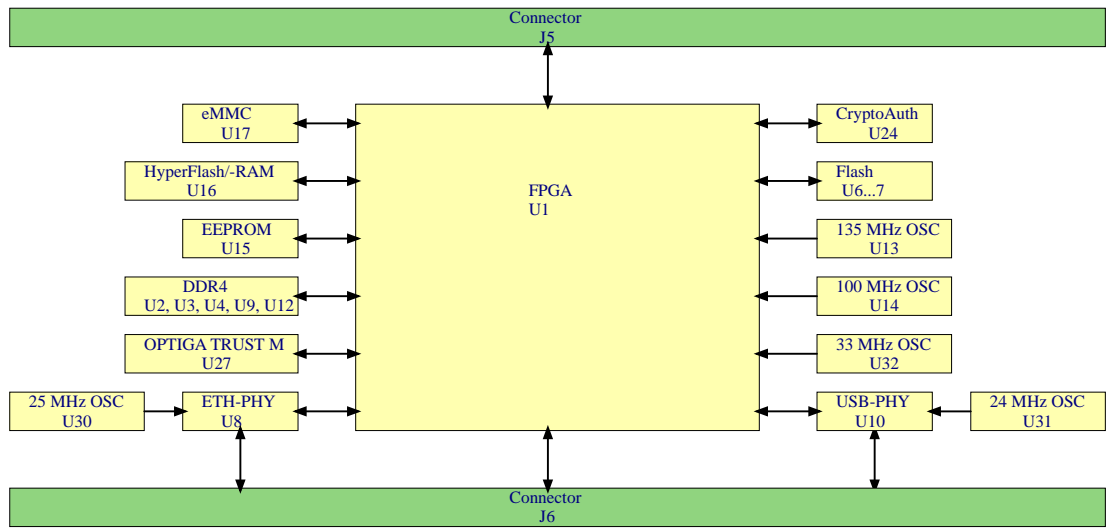
Schematics and other handouts serve for informational purposes only!

	Title: <b>AM0010 – Legal Notices Modules</b>		
	A4	Number: <b>Legal Notices Modules [No Variations]</b>	Rev. <b>02</b>
	Date: <b>22.07.2022</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>1</b> of <b>30</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

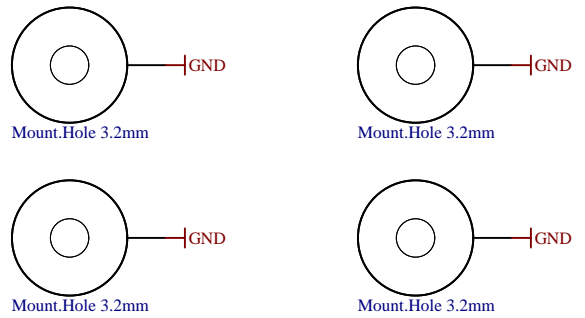
- U\_B2B\_Connector\_1  
B2B\_Connector\_1.SchDoc
- U\_B2B\_Connector\_2  
B2B\_Connector\_2.SchDoc
- U\_MPSoC  
MPSoC.SchDoc
- U\_DDR4-RAM  
DDR4-RAM.SchDoc
- U\_DDR4-RAM\_2  
DDR4-RAM\_2.SchDoc
- U\_DDR4-RAM\_3  
DDR4-RAM\_3.SchDoc
- U\_DDR4-RAM\_4  
DDR4-RAM\_4.SchDoc
- U\_DDR4-RAM\_5  
DDR4-RAM\_5.SchDoc
- U\_DDR4-CAPS  
DDR4-CAPS.SchDoc
- U\_DDR4-TERM  
DDR4-TERM.SchDoc
- U\_ETHPHY  
ETHPHY.SchDoc
- U\_USBPHY  
USBPHY.SchDoc
- U\_eMMC  
eMMC.SchDoc
- U\_MISC  
MISC.SchDoc

- U\_POWER\_1  
POWER\_1.SchDoc
- U\_POWER\_2  
POWER\_2.SchDoc
- U\_REV\_CH  
Revision\_Changes.SchDoc
- U\_Legal\_Notices\_Modules  
Legal\_Notices\_Modules.SchDoc

Special notes:



Serial  
Serialnumber 6,3 x 6.3mm



UKCA  
UKCA Logo on Top Overlay  
UKCA-TOPOVERLAY



Assembly variant	[No Variations]
Created by	
Modified by	
Modified at	
SVN Revision	588

Title: AM0010		
A4	Number: AM0010 [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 2 of 30
Filename: AM0010.SchDoc		

1

2

3

4

A

A

B

B

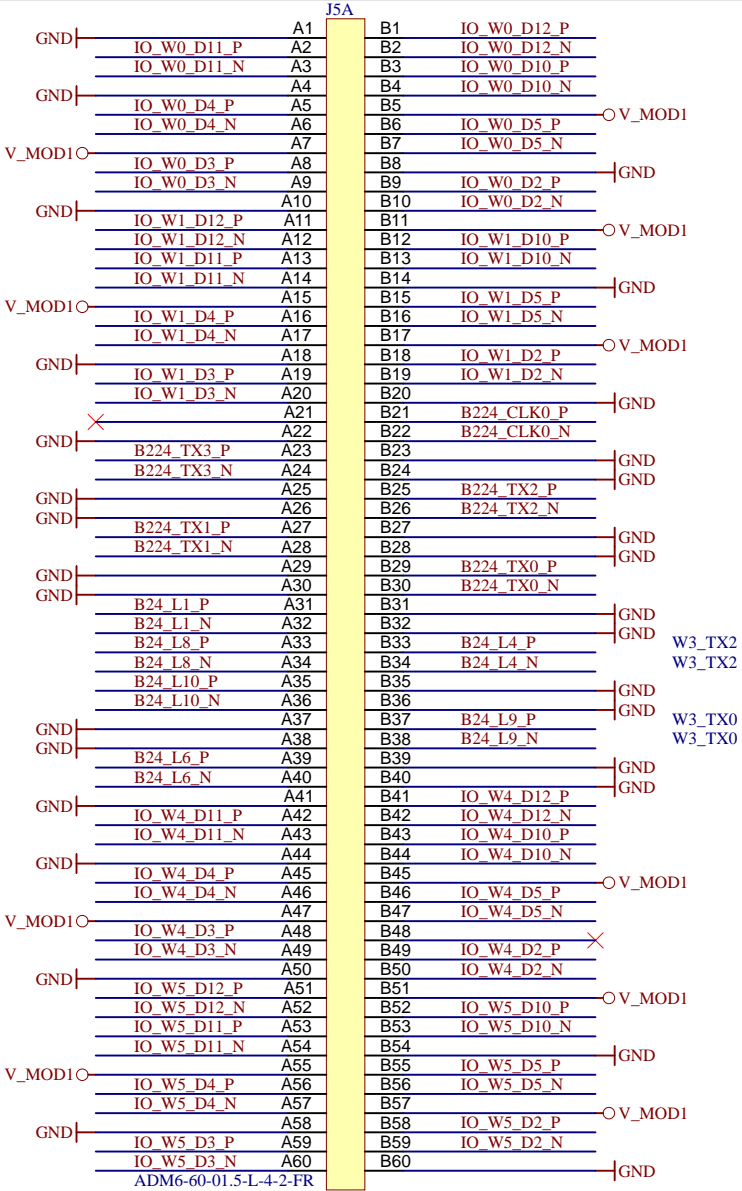
C

C

D

D

Connector W

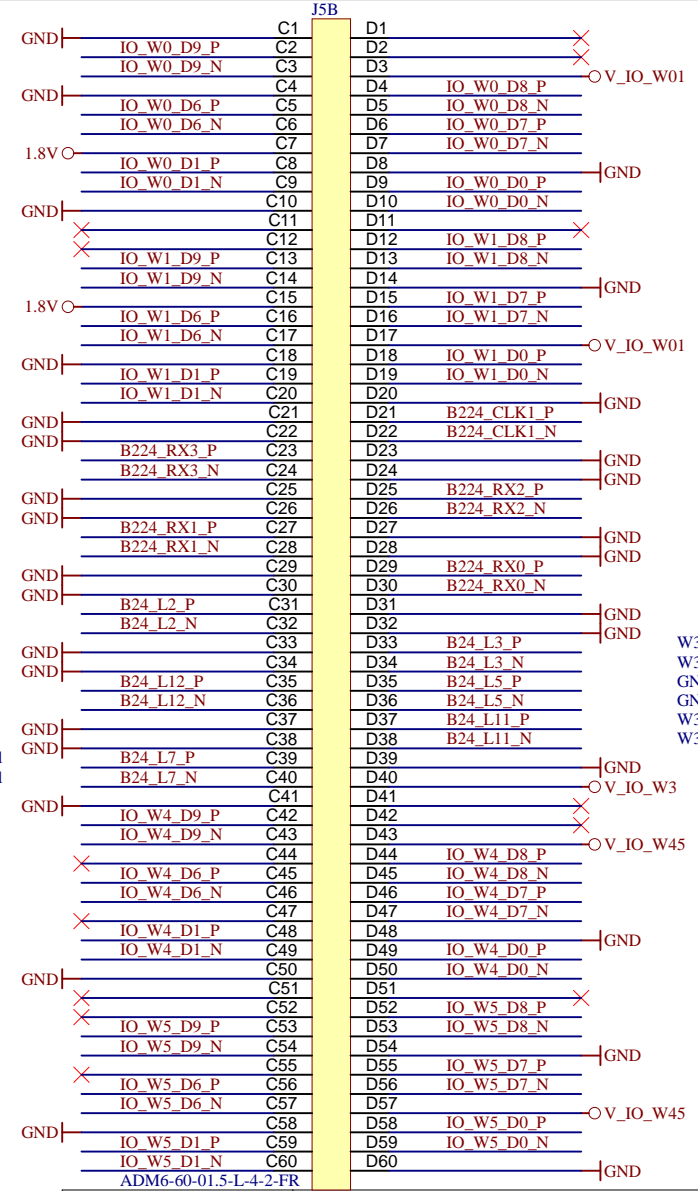


W3\_TX3  
W3\_TX3  
GND  
W3\_TX1  
W3\_TX1

W3\_CLK0  
W3\_CLK0

W3\_TX2  
W3\_TX2

W3\_TX0  
W3\_TX0



W3\_RX3  
W3\_RX3

W3\_RX1  
W3\_RX1

W3\_CLK1  
W3\_CLK1

V\_IO\_W01

V\_IO\_W01

W3\_RX2  
W3\_RX2  
GND  
W3\_RX0  
W3\_RX0

V\_IO\_W3

V\_IO\_W45

V\_IO\_W45



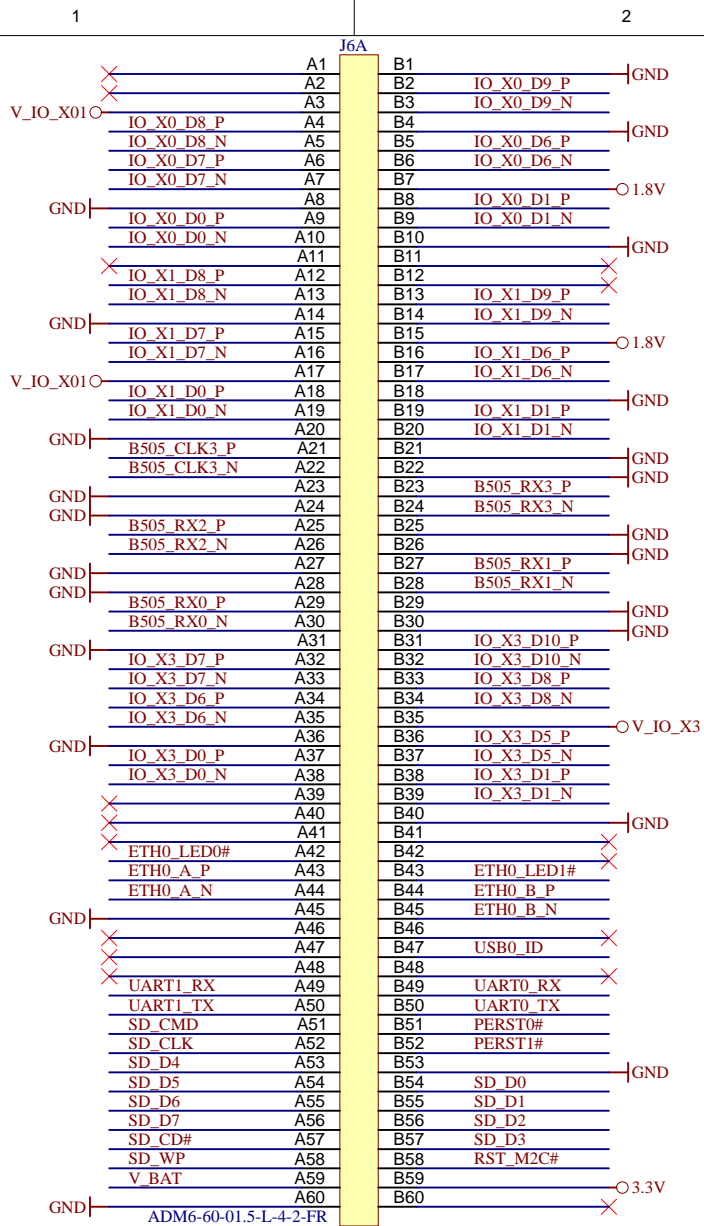
Title: AM0010 – B2B_Connector_1		
A4	Number: B2B_Connector_1 [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 3 of 30
Filename: B2B_Connector_1.SchDoc		

1

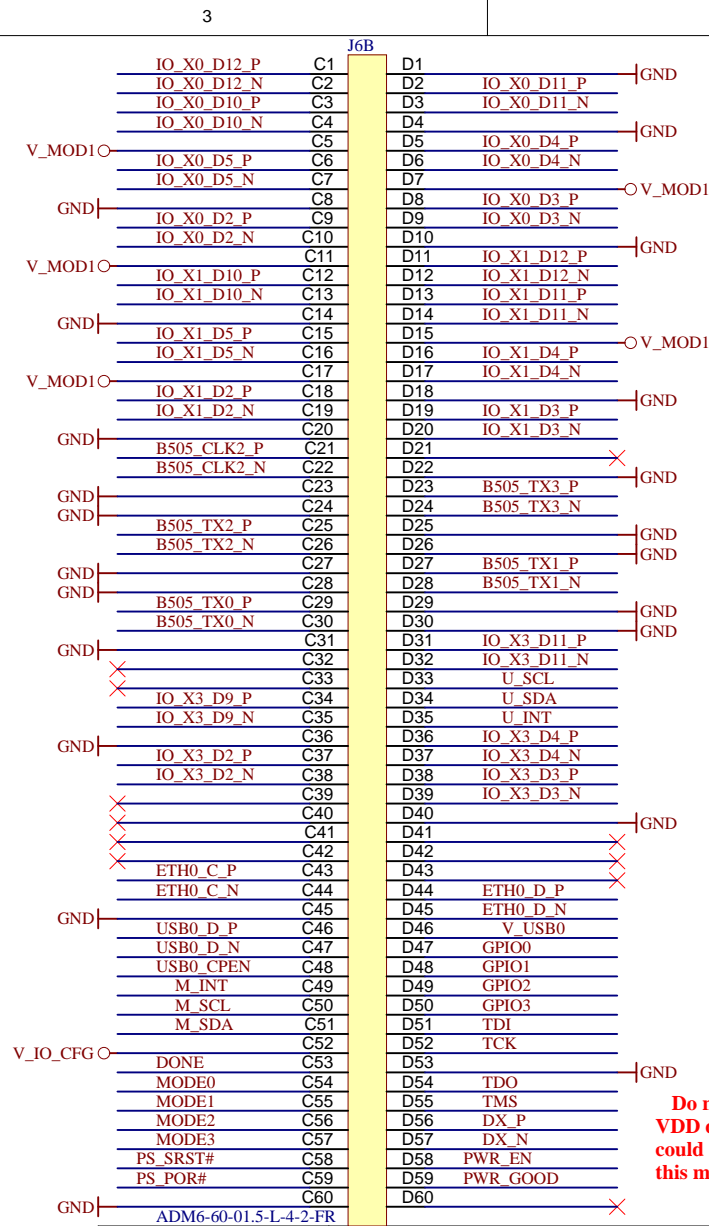
2

3

4



Connector X



**Do not tie "PWR\_EN" to VDD directly. This signal could be tied to GND within this module.**



Title: <b>AM0010 - B2B_Connector_2</b>		
A4	Number: <b>B2B_Connector_2</b> [No Variations]	Rev. <b>02</b>
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 4 of 30
Filename: <b>B2B_Connector_2.SchDoc</b>		



1

2

3

4

A

A

- U\_B64  
B64.SchDoc
- U\_B65  
B65.SchDoc
- U\_B66  
B66.SchDoc
- U\_B\_HD  
B\_HD.SchDoc
- U\_B\_MIO  
B\_MIO.SchDoc
- U\_PS\_DDR  
PS\_DDR.SchDoc
- U\_B\_PS\_GT  
B\_PS\_GT.SchDoc
- U\_B\_GT  
B\_GT.SchDoc
- U\_CONFIG  
CONFIG.SchDoc
- U\_ZU\_POWER  
ZU\_POWER.SchDoc
- U\_ZU\_PS\_POWER  
ZU\_PS\_POWER.SchDoc

B


B

C

C

D

D

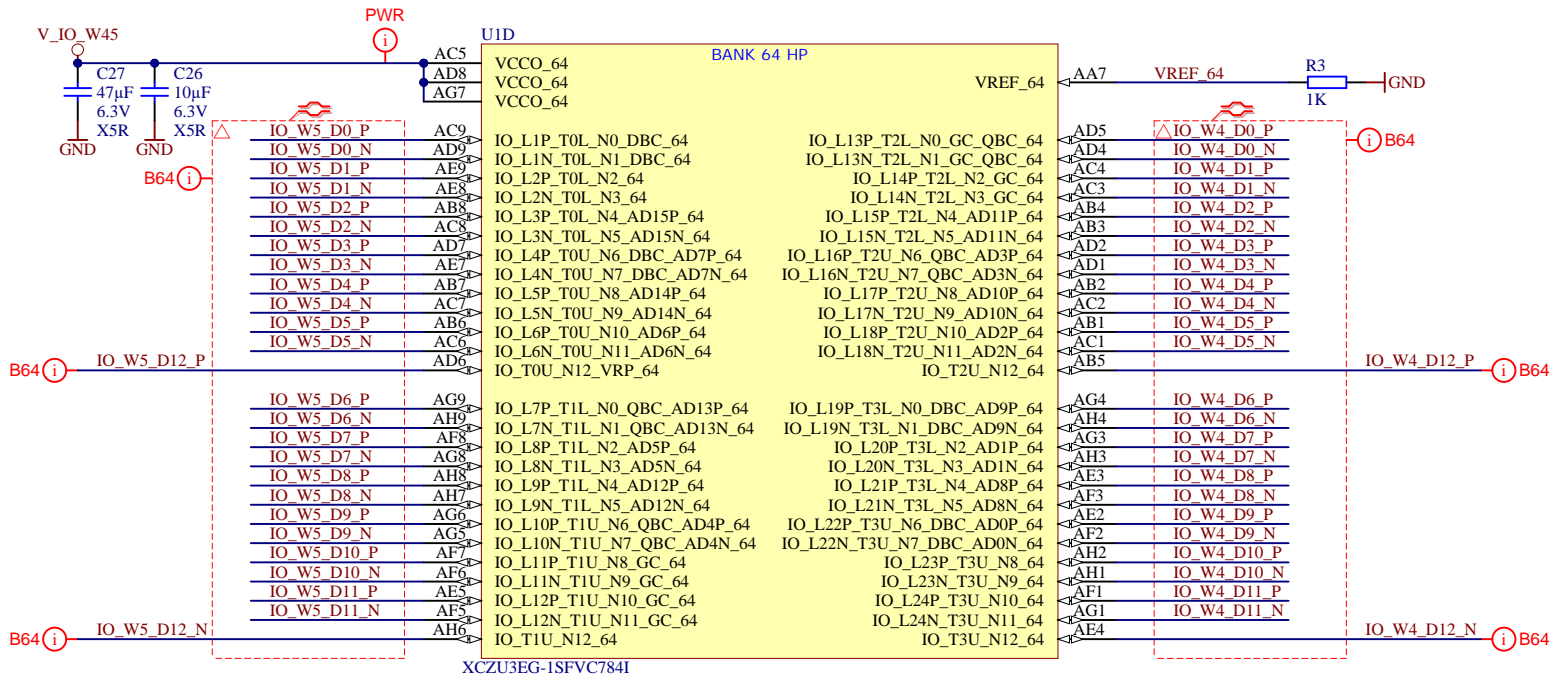
	Title: AM0010 – MPSoC		
	A4	Number: MPSoC [No Variations]	Rev. 02
	Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 5 of 30
	Filename: MPSoC.SchDoc		

1

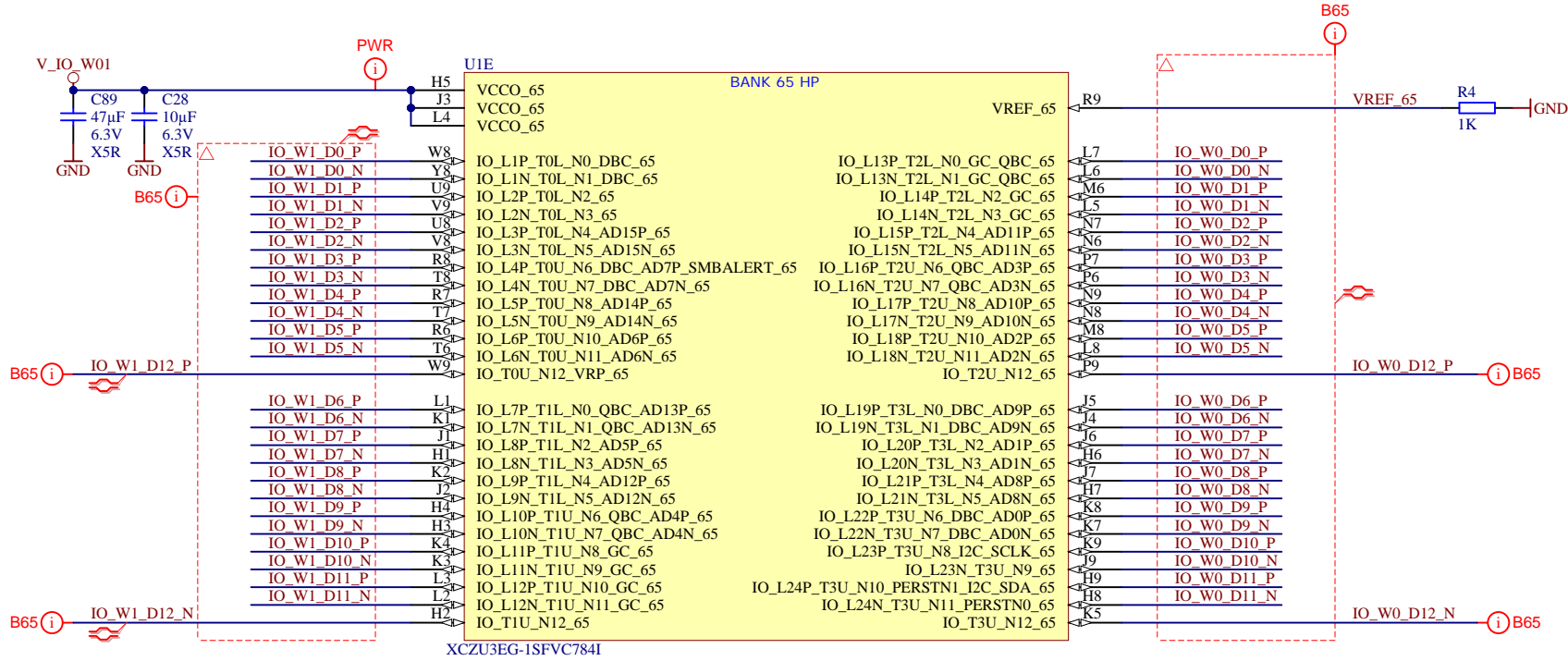
2

3

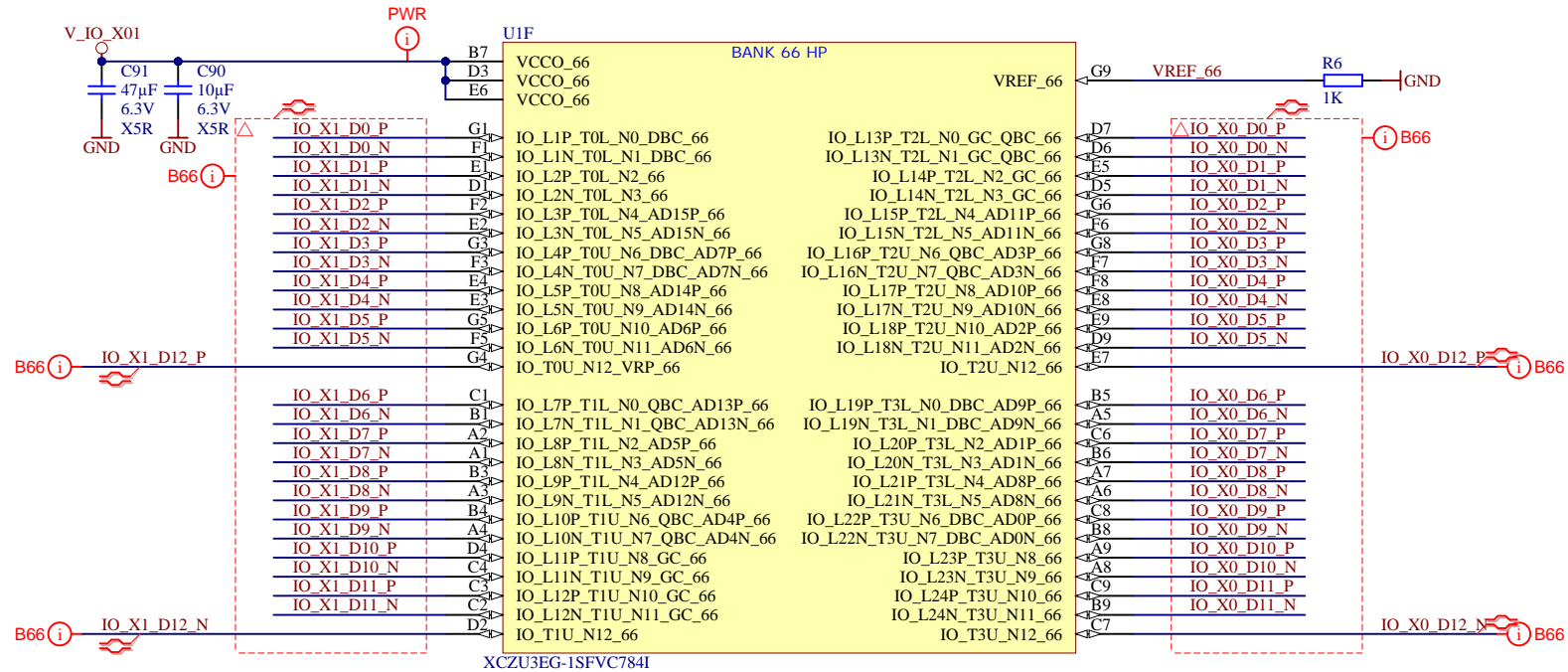
4




Title: AM0010 – B64		
A4	Number: B64 [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 6 of 30
Filename: B64.SchDoc		



Title: AM0010 – B65		
A4	Number: B65 [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 7 of 30
Filename: B65.SchDoc		



			Title: AM0010 – B66	
			A4	Number: B66 [No Variations]
Date: 22.07.2022		Copyright: Trenz Electronic GmbH		Page 8 of 30
Filename: B66.SchDoc				

A

A

B

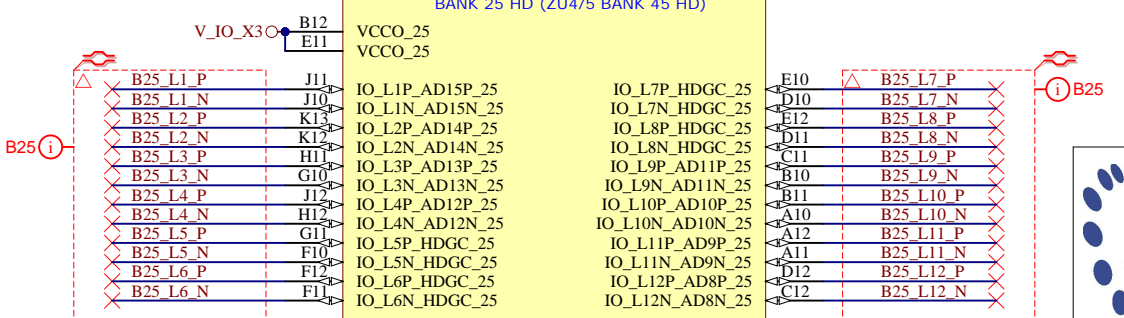
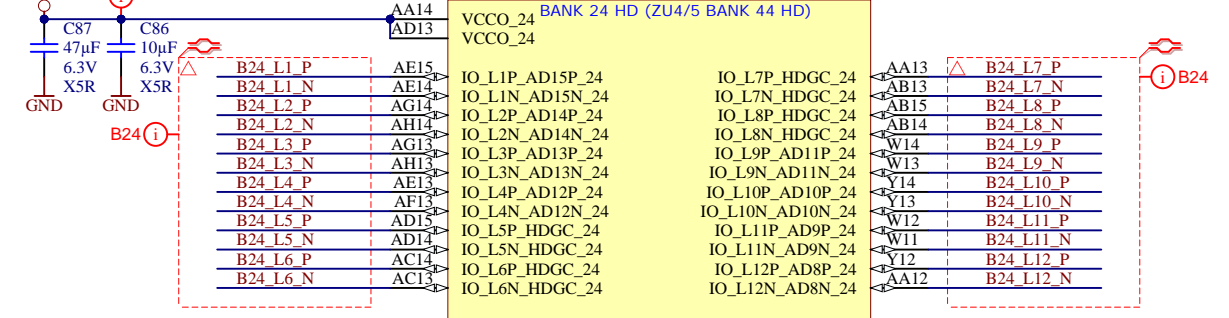
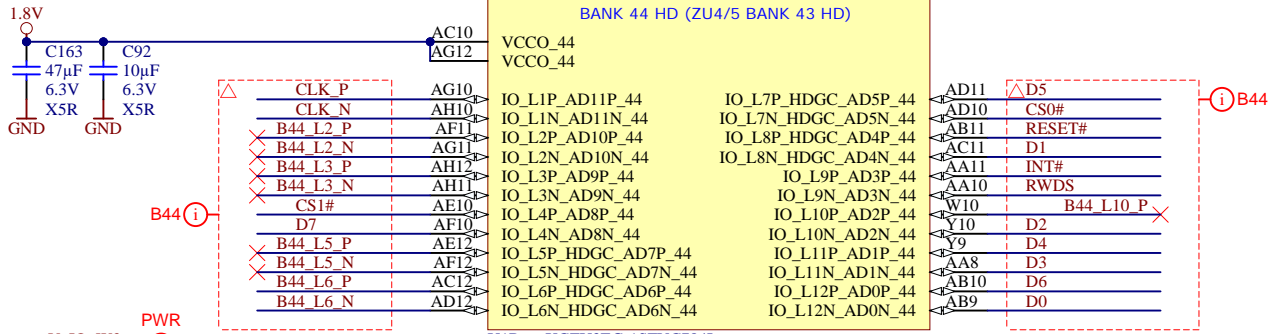
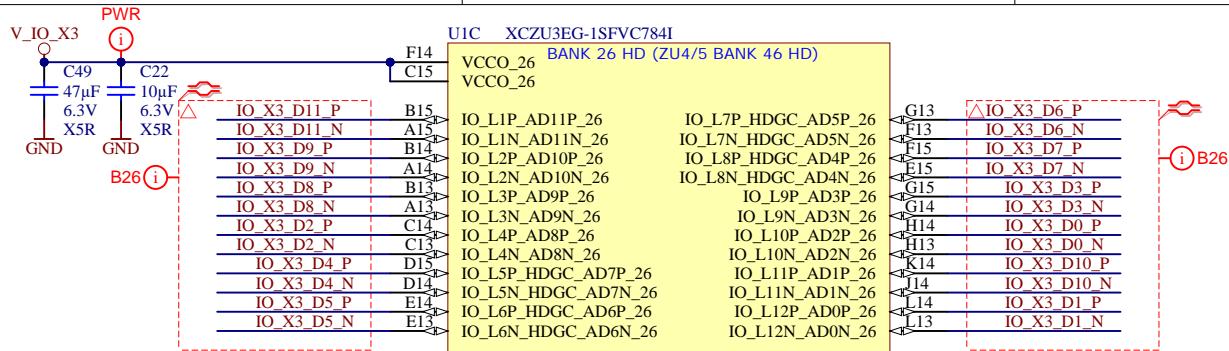
B

C

C

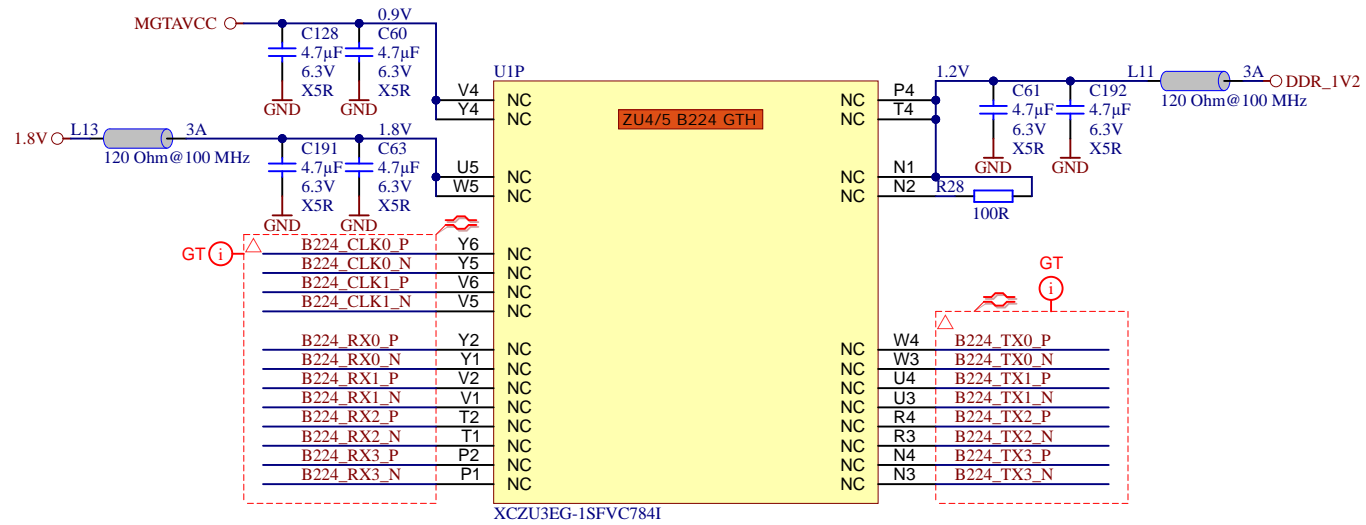
D


D

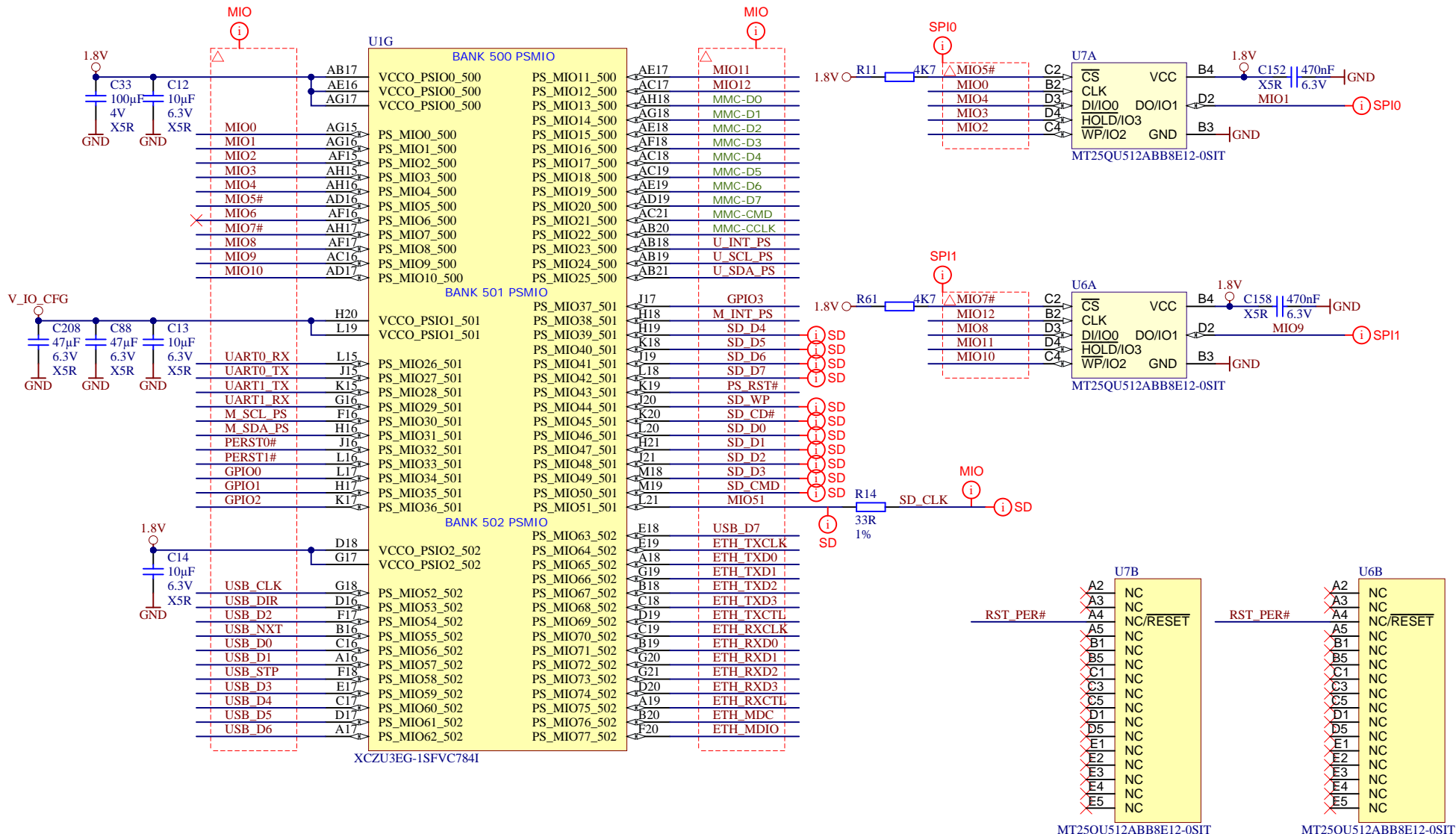



Title: AM0010 - B_HD		
A4	Number: B_HD [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 9 of 30
Filename: B_HD.SchDoc		

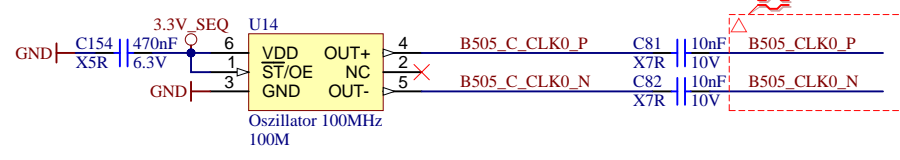
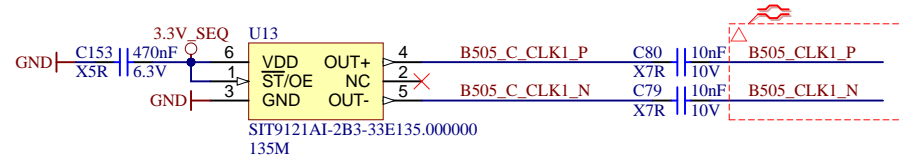
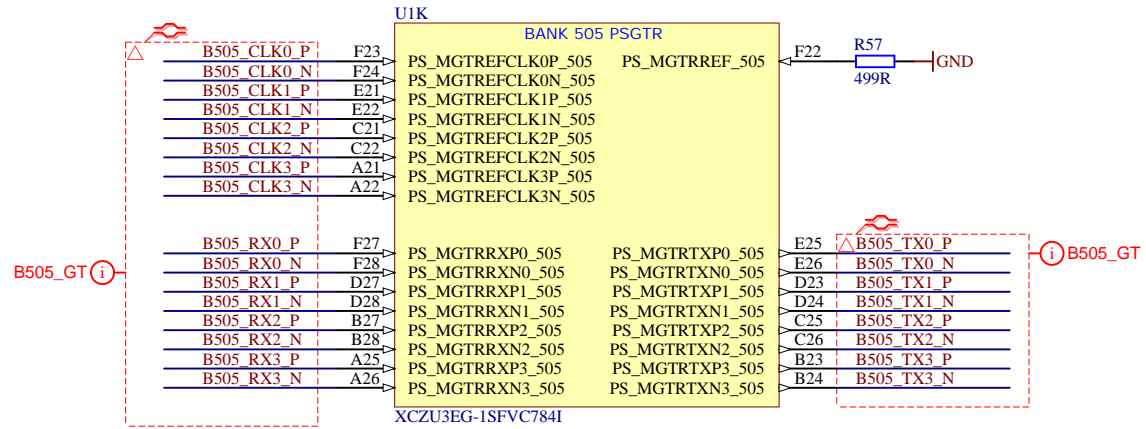




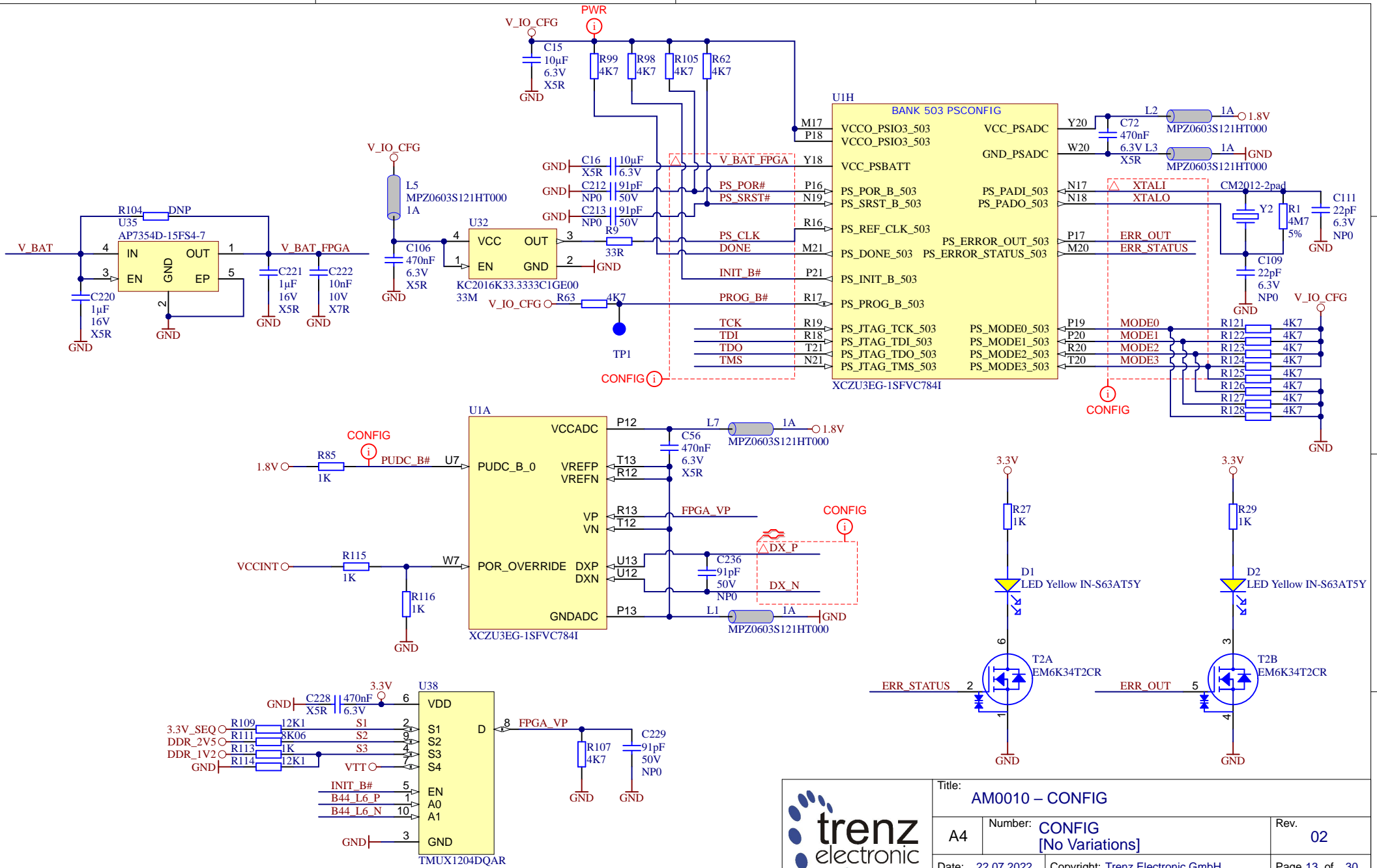
	Title: AM0010 – B_GT		
	A4	Number: B_GT [No Variations]	Rev. 02
	Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 10 of 30
	Filename: B_GT.SchDoc		



		Title: AM0010 - B_MIO	
		A4	Number: B_MIO [No Variations]
Date: 22.07.2022		Copyright: Trenz Electronic GmbH	
Filename: B_MIO.SchDoc		Page 11 of 30	



	Title: AM0010 – B_PS_GT		
	A4	Number: B_PS_GT [No Variations]	Rev. 02
	Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 12 of 30
	Filename: B_PS_GT.SchDoc		



Title: AM0010 – CONFIG		
A4	Number: CONFIG [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 13 of 30
Filename: CONFIG.SchDoc		

A

A

B

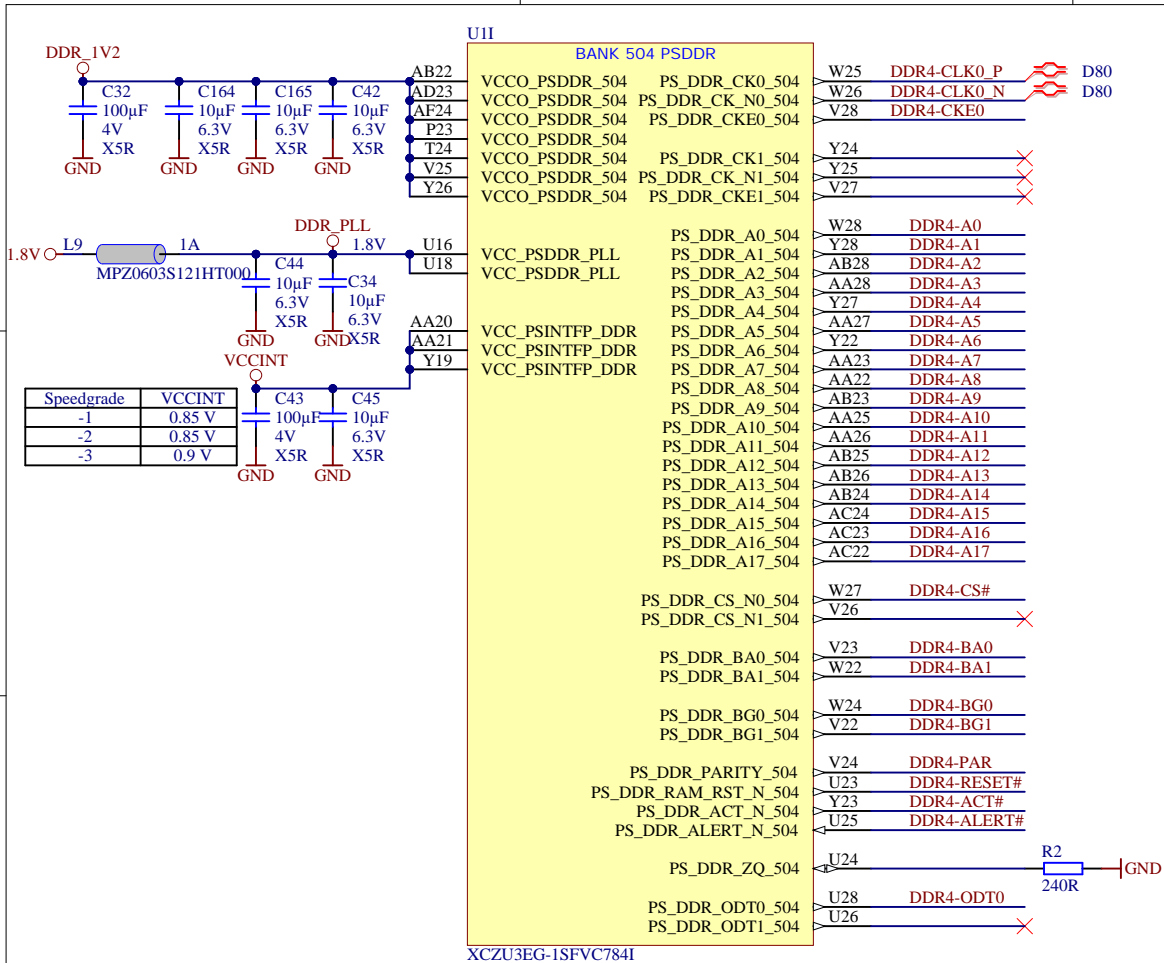
B

C

C

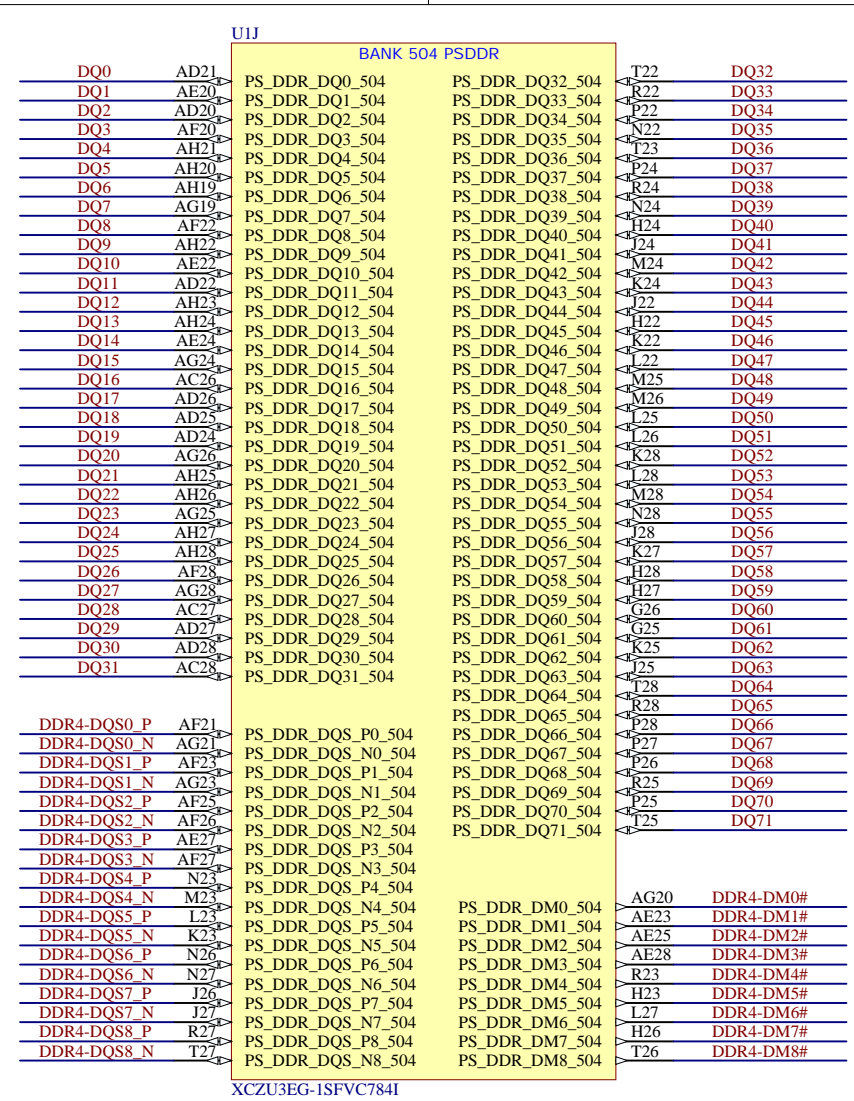
D

D



XCU3EG-1SFVC784I

U11 BANK 504 PSDDR		U1J BANK 504 PSDDR	
VCC0_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0_P
VCC0_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0_N
VCC0_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCC0_PSDDR_504	PS_DDR_CK1_504	Y24	
VCC0_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCC0_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AC22	DDR4-A17
PS_DDR_CS_N0_504	PS_DDR_CS_N1_504	W27	DDR4-CS#
PS_DDR_CS_N0_504	PS_DDR_CS_N1_504	V26	
PS_DDR_BA0_504	PS_DDR_BA1_504	V23	DDR4-BA0
PS_DDR_BA0_504	PS_DDR_BA1_504	W22	DDR4-BA1
PS_DDR_BG0_504	PS_DDR_BG1_504	W24	DDR4-BG0
PS_DDR_BG0_504	PS_DDR_BG1_504	V22	DDR4-BG1
PS_DDR_PARITY_504	PS_DDR_RAM_RST_N_504	V24	DDR4-PAR
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	U23	DDR4-RESET#
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	Y23	DDR4-ACT#
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	U25	DDR4-ALERT#
PS_DDR_ZQ_504	PS_DDR_ODT0_504	U24	DDR4-ZQ
PS_DDR_ODT0_504	PS_DDR_ODT1_504	U28	DDR4-ODT0
PS_DDR_ODT0_504	PS_DDR_ODT1_504	U26	



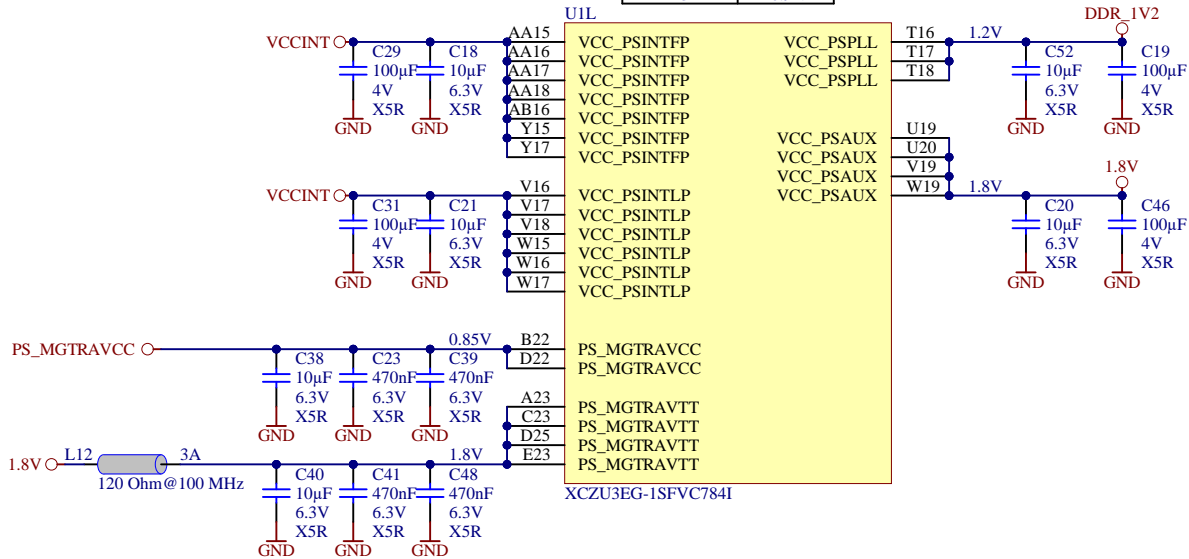
XCU3EG-1SFVC784I




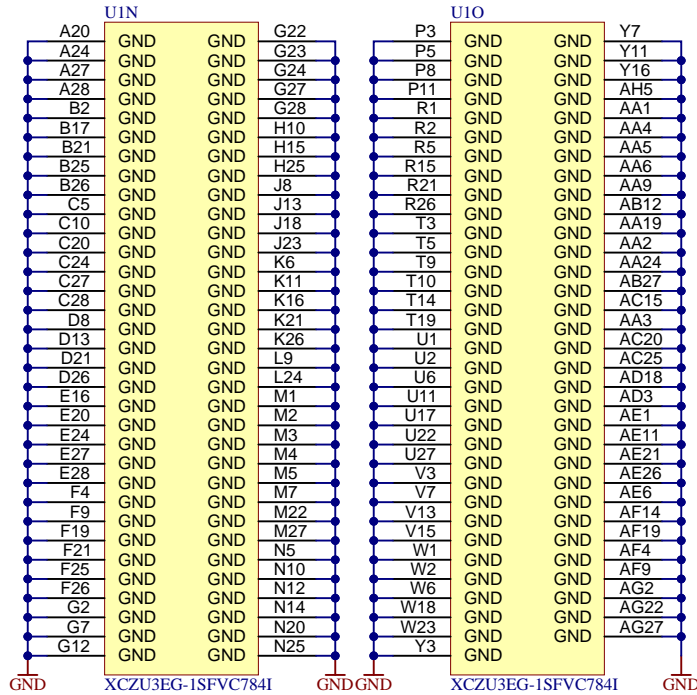
Title: AM0010 – PS_DDR		
A4	Number: PS_DDR [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 14 of 30
Filename: PS_DDR.SchDoc		



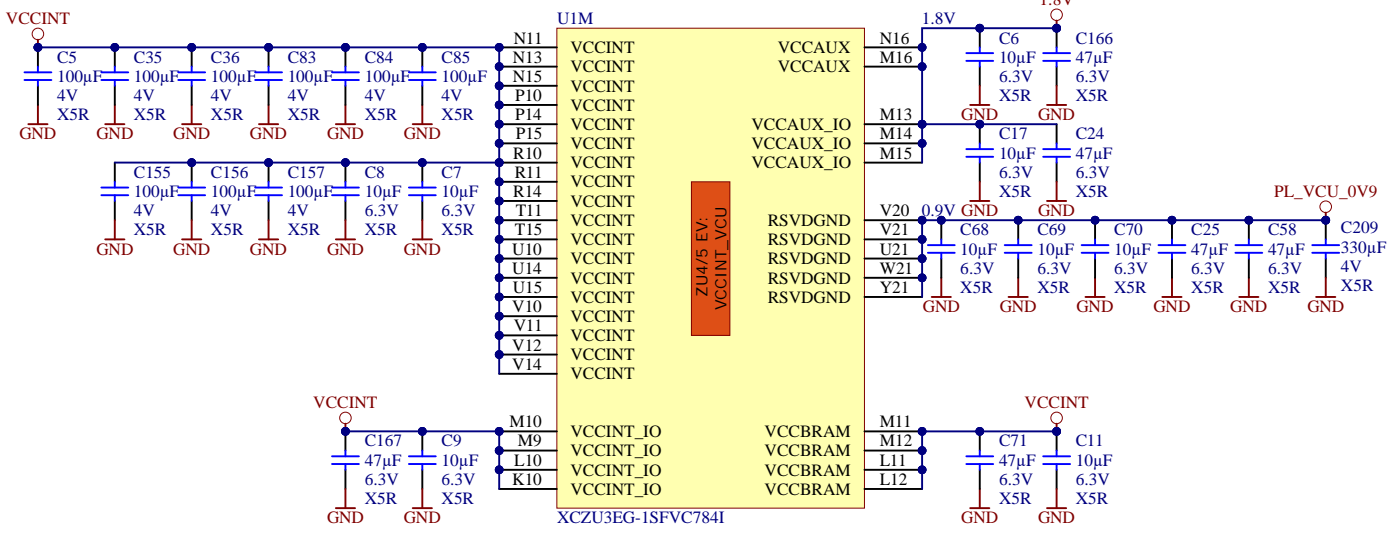

Speedgrade	VCCINT
-1	0.85 V
-2	0.85 V
-3	0.9 V



	Title: AM0010 – ZU_PS_POWER		
	A4	Number: ZU_PS_POWER [No Variations]	Rev. 02
	Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 15 of 30
	Filename: ZU_PS_POWER.SchDoc		

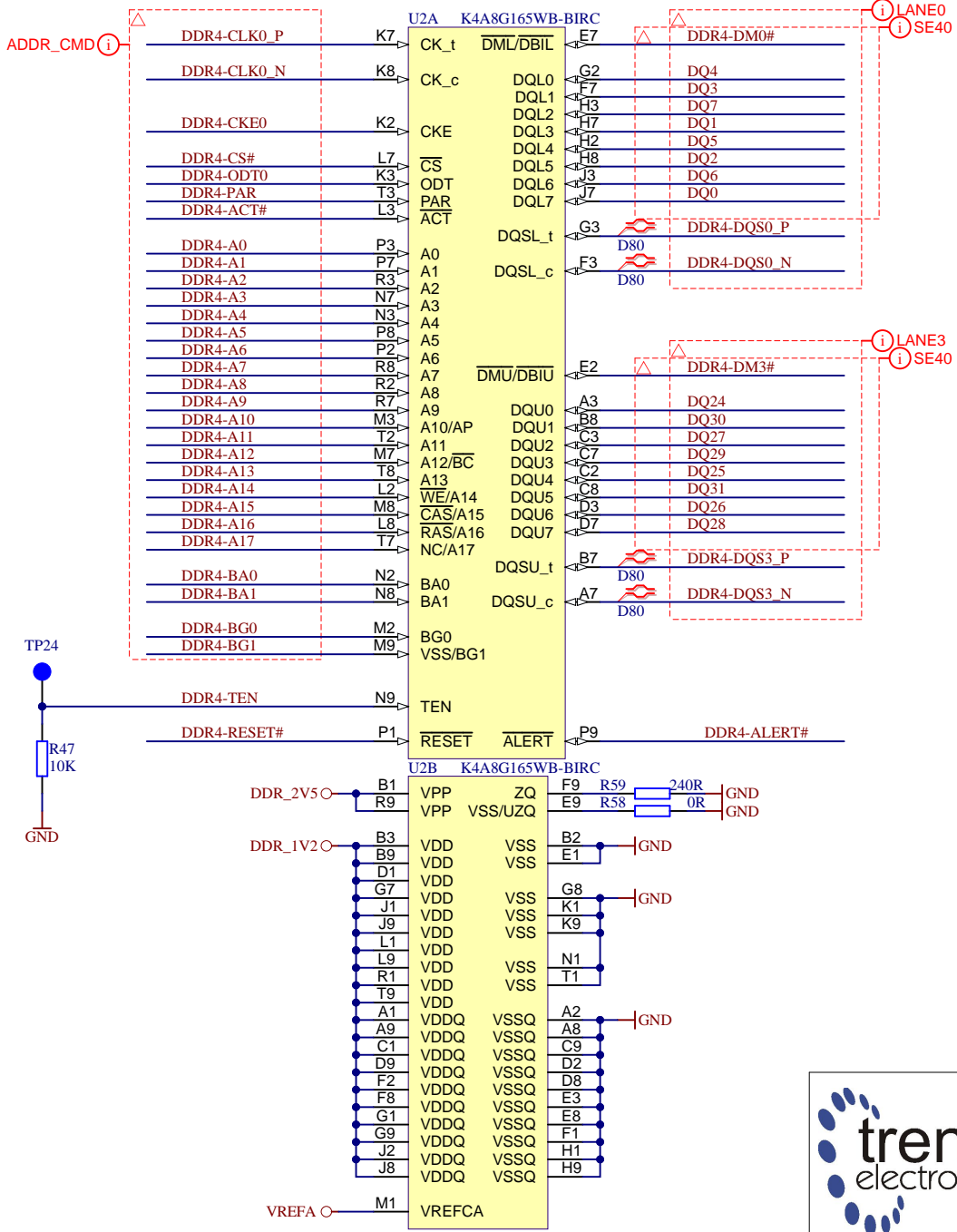


Speedgrade	VCCINT
-1	0.85 V
-2	0.85 V
-3	0.9 V

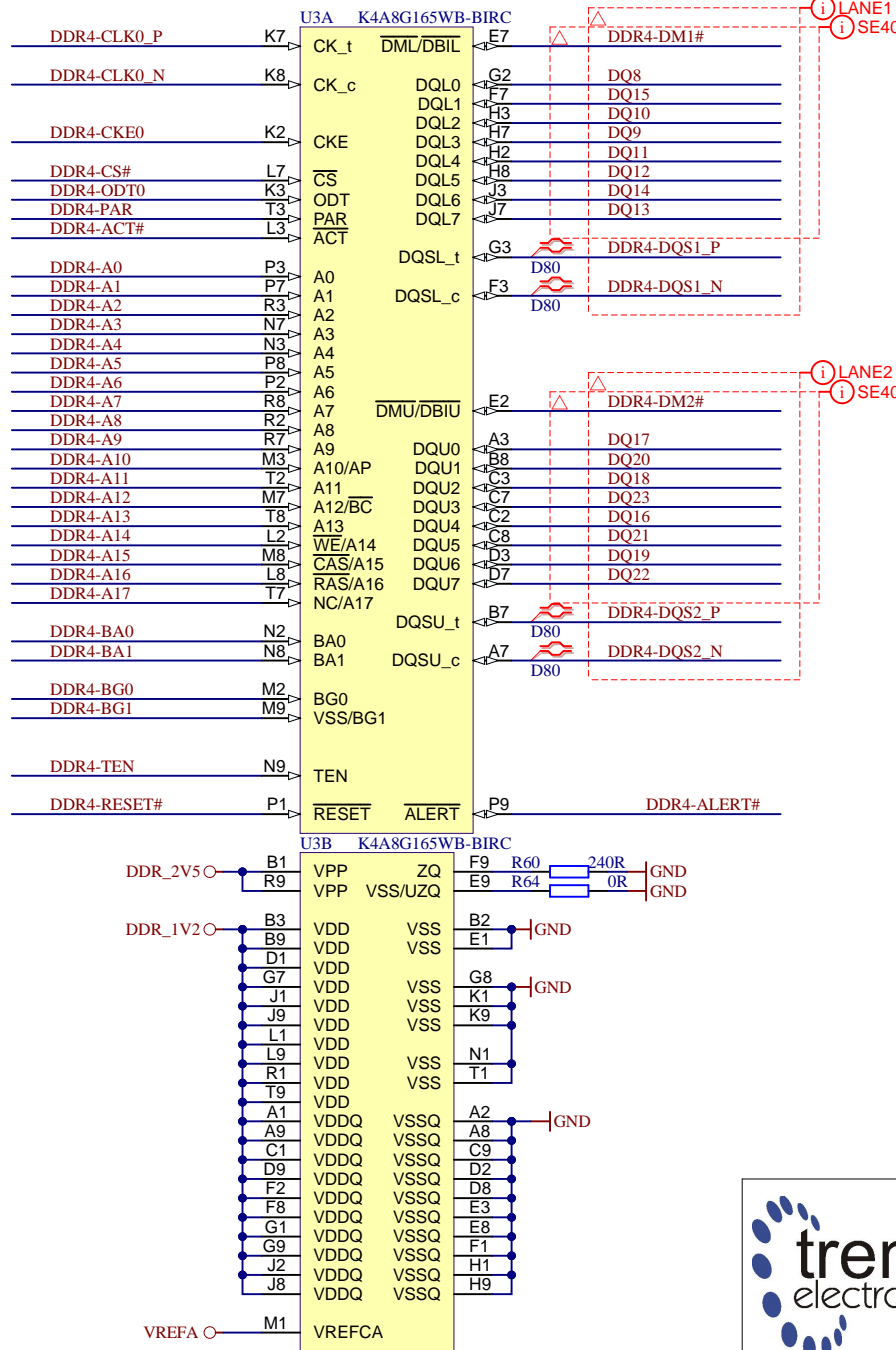




**trenz electronic**

Title: AM0010 – ZU_POWER		
A4	Number: ZU_POWER [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 16 of 30
Filename: ZU_POWER.SchDoc		



Title: AM0010 – DDR4-RAM		
A4	Number: DDR4-RAM [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 17 of 30
Filename: DDR4-RAM.SchDoc		



		Title: AM0010 – DDR4-RAM_2	
		A4	Number: DDR4-RAM_2 [No Variations]
Date: 22.07.2022		Copyright: Trenz Electronic GmbH	
Filename: DDR4-RAM_2.SchDoc		Page 18 of 30	

A

A

B

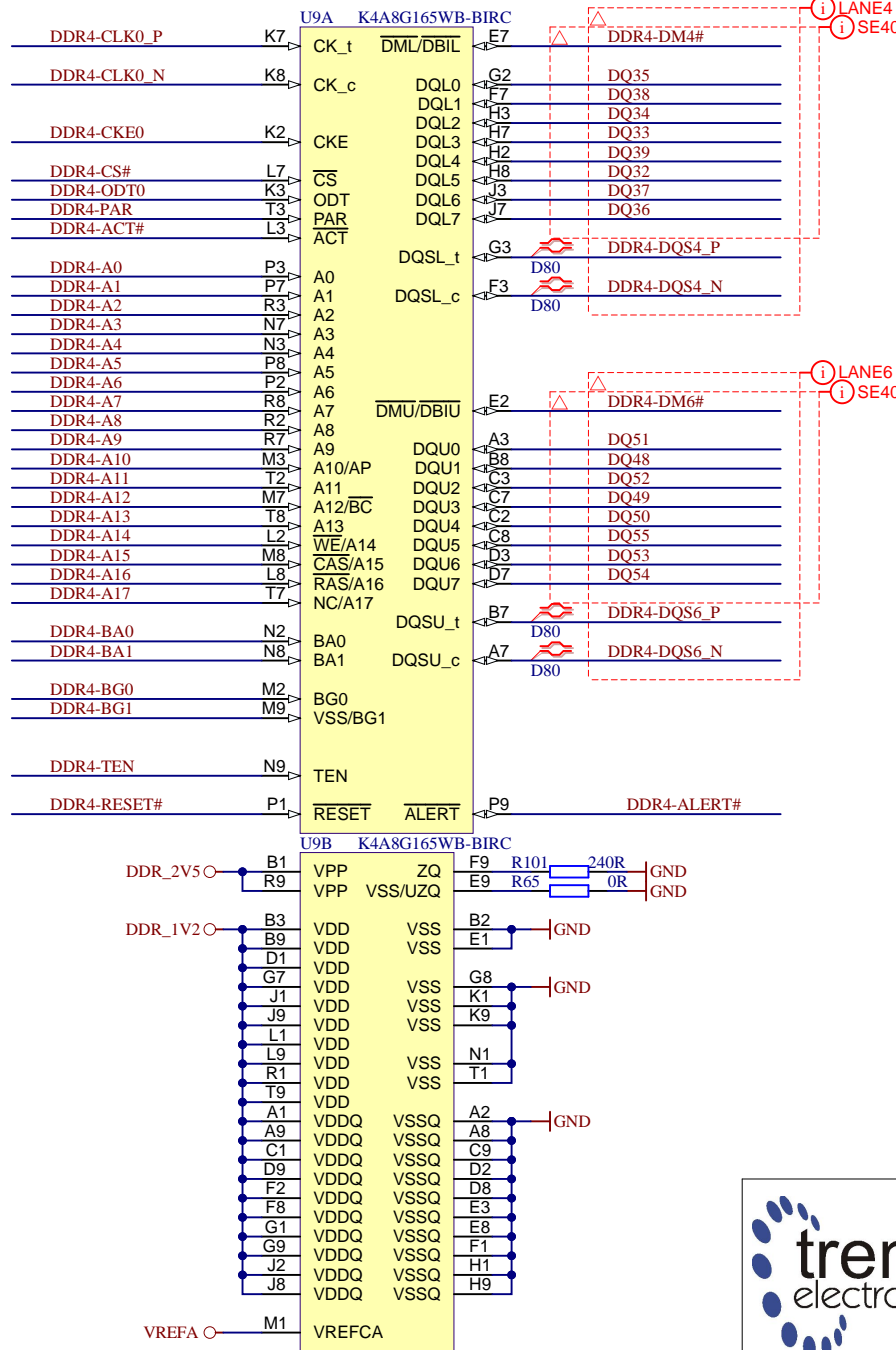
B


C

C

D

D



		Title: AM0010 – DDR4-RAM_3	
		A4	Number: DDR4-RAM_3 [No Variations]
Date: 22.07.2022		Copyright: Trenz Electronic GmbH	
Filename: DDR4-RAM_3.SchDoc		Page 19 of 30	



A

A

B

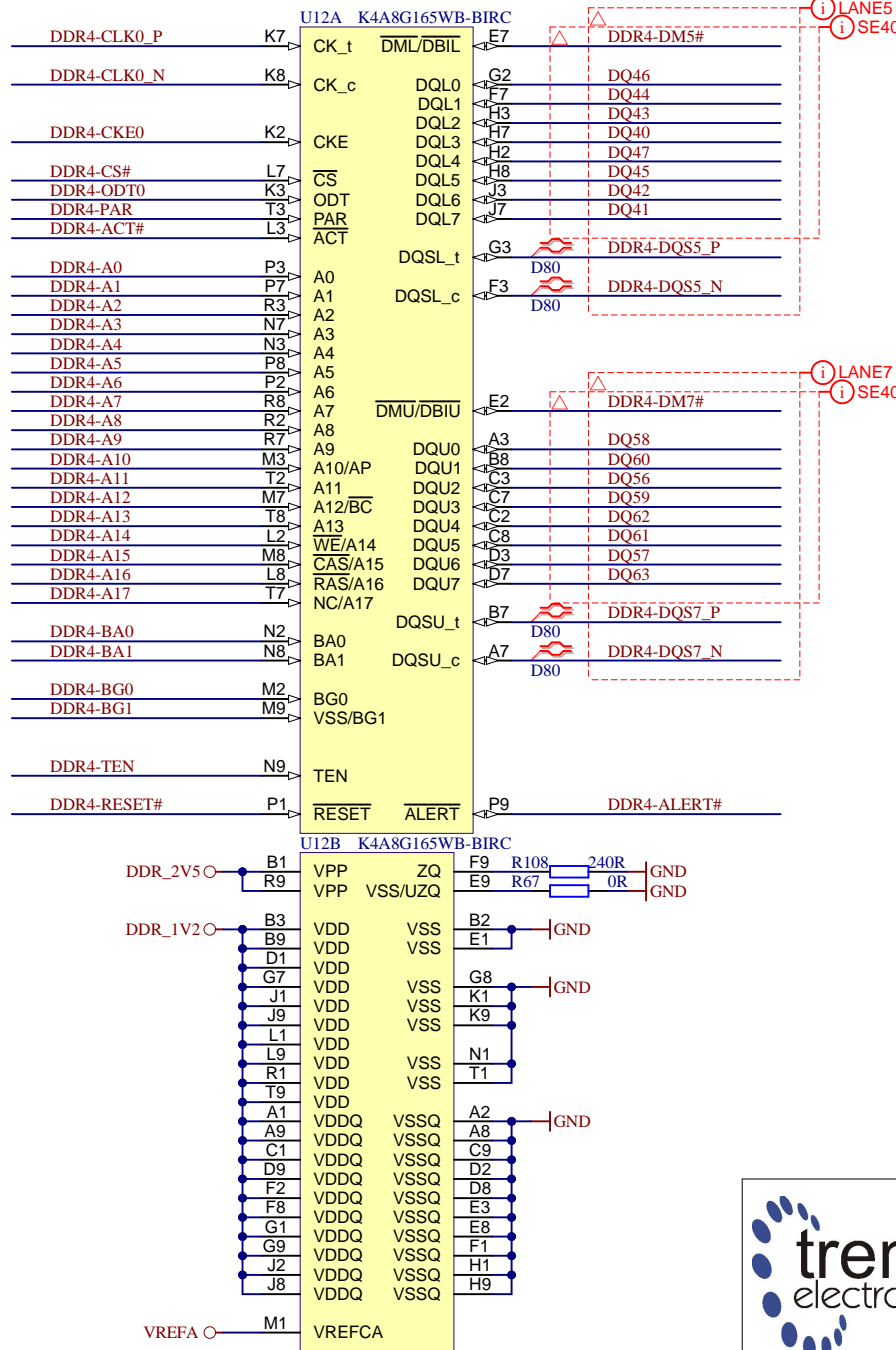

B

C

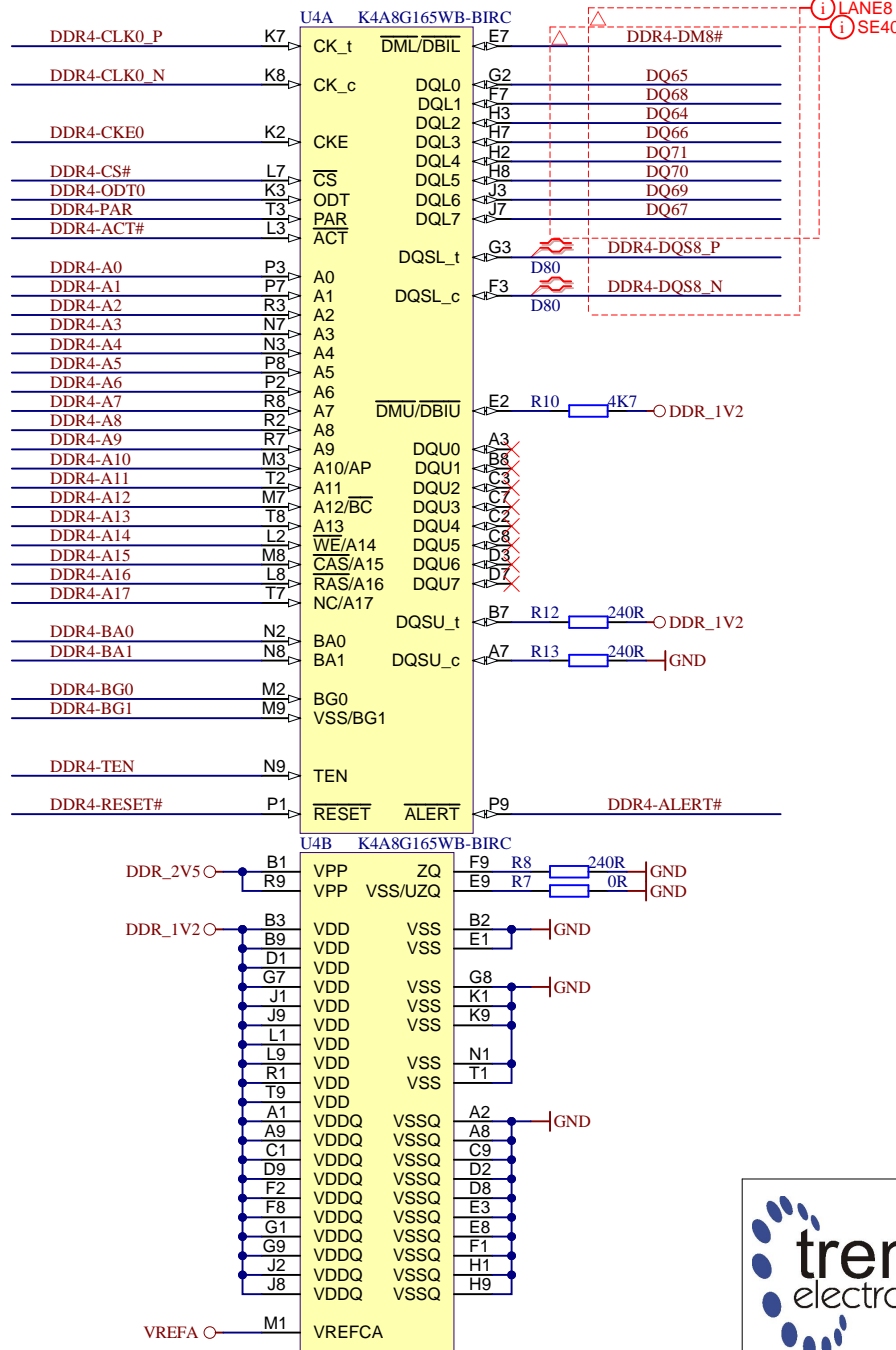
C

D

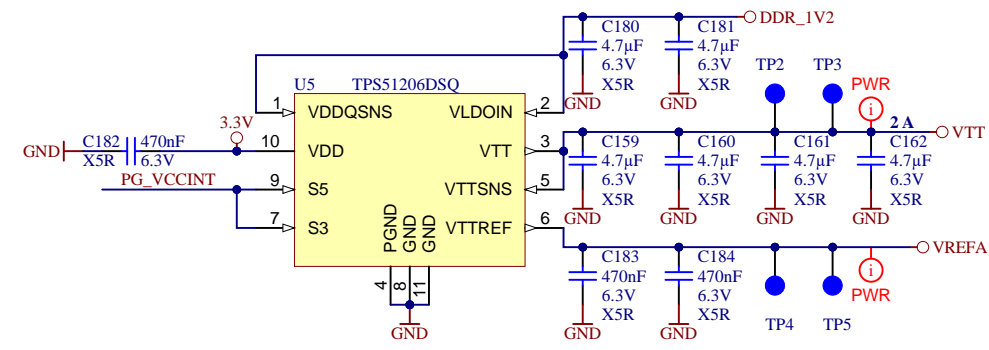
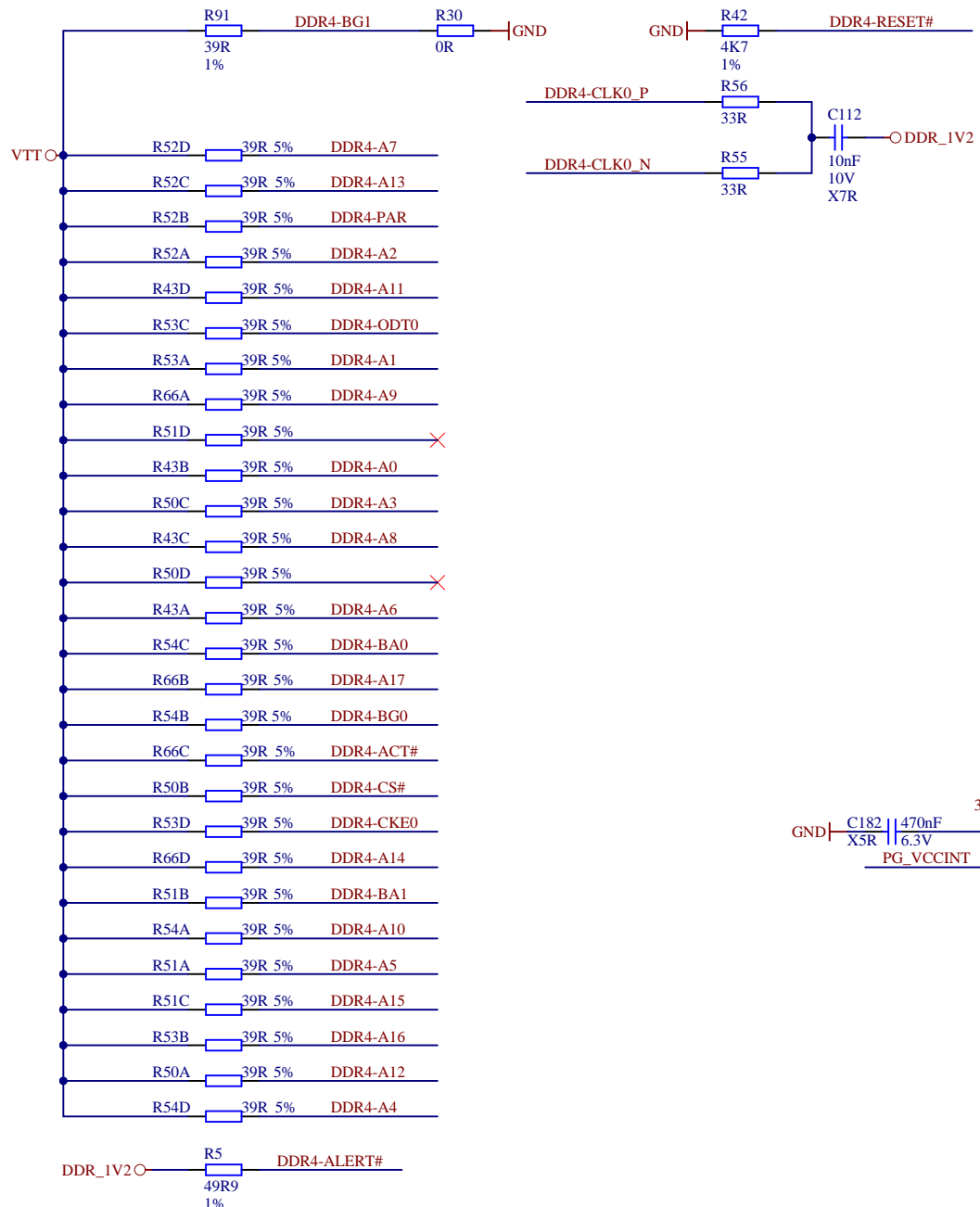
D

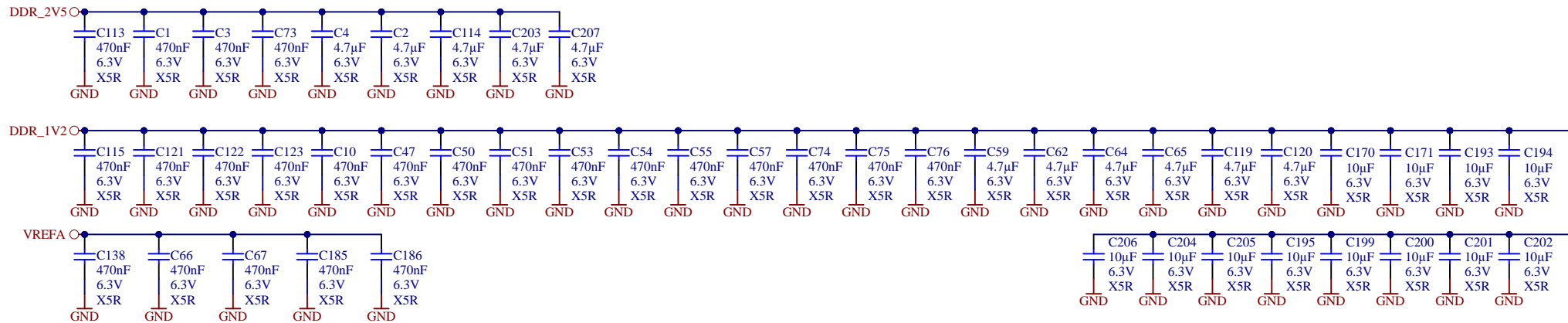
Title: AM0010 – DDR4-RAM_4		
A4	Number: DDR4-RAM_4 [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 20 of 30
Filename: DDR4-RAM_4.SchDoc		



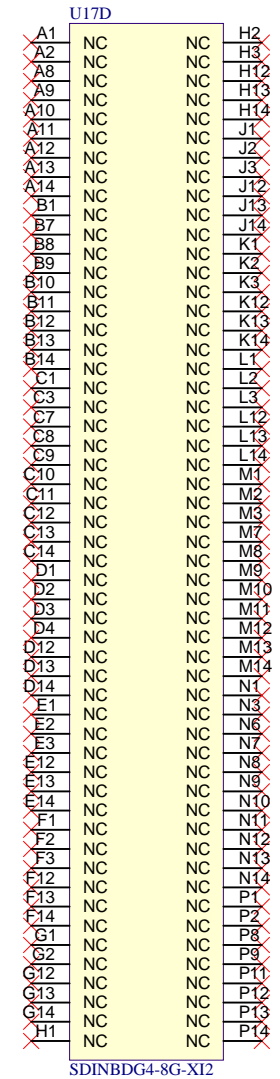
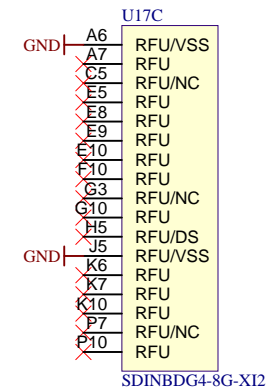
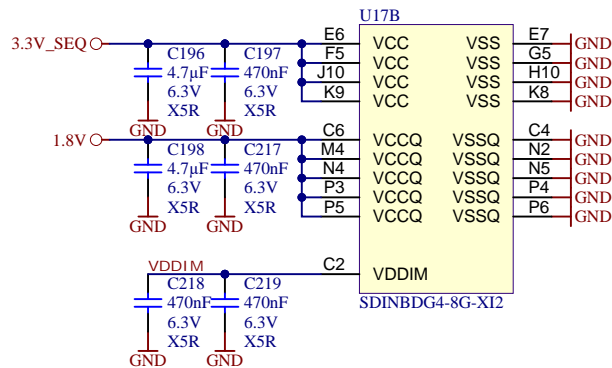
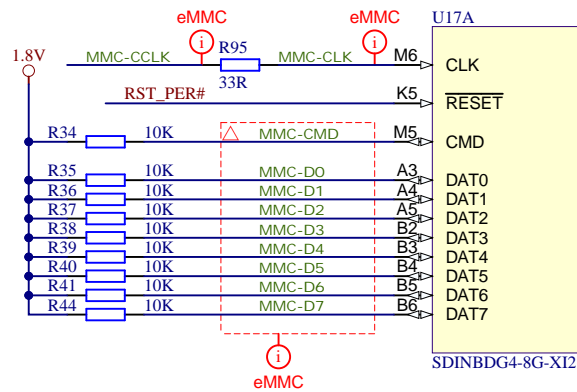
Title: AM0010 – DDR4-RAM_5		
A4	Number: DDR4-RAM_5 [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 21 of 30
Filename: DDR4-RAM_5.SchDoc		



Title: AM0010 – DDR4-TERM		
A4	Number: DDR4-TERM [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 22 of 30
Filename: DDR4-TERM.SchDoc		

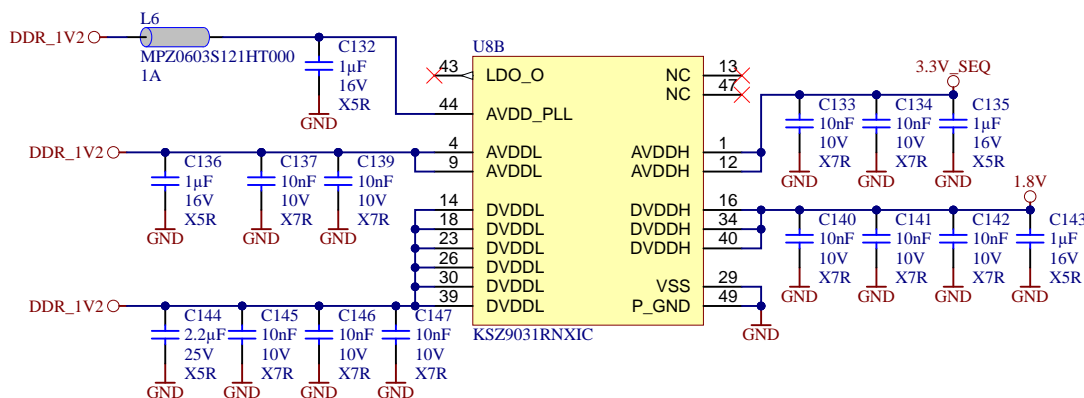
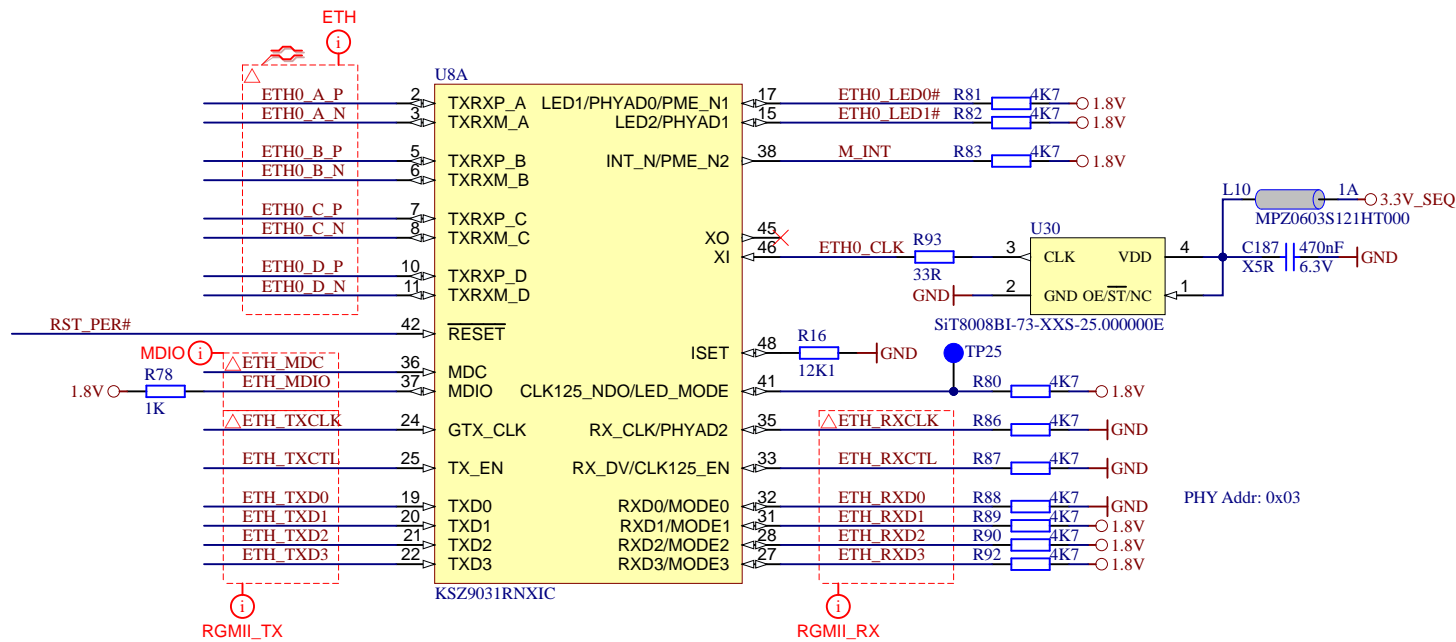


Title: AM0010 – DDR4-CAPS		
A4	Number: DDR4-CAPS [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 23 of 30
Filename: DDR4-CAPS.SchDoc		



Title: AM0010 – eMMC		
A4	Number: eMMC [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 24 of 30
Filename: eMMC.SchDoc		

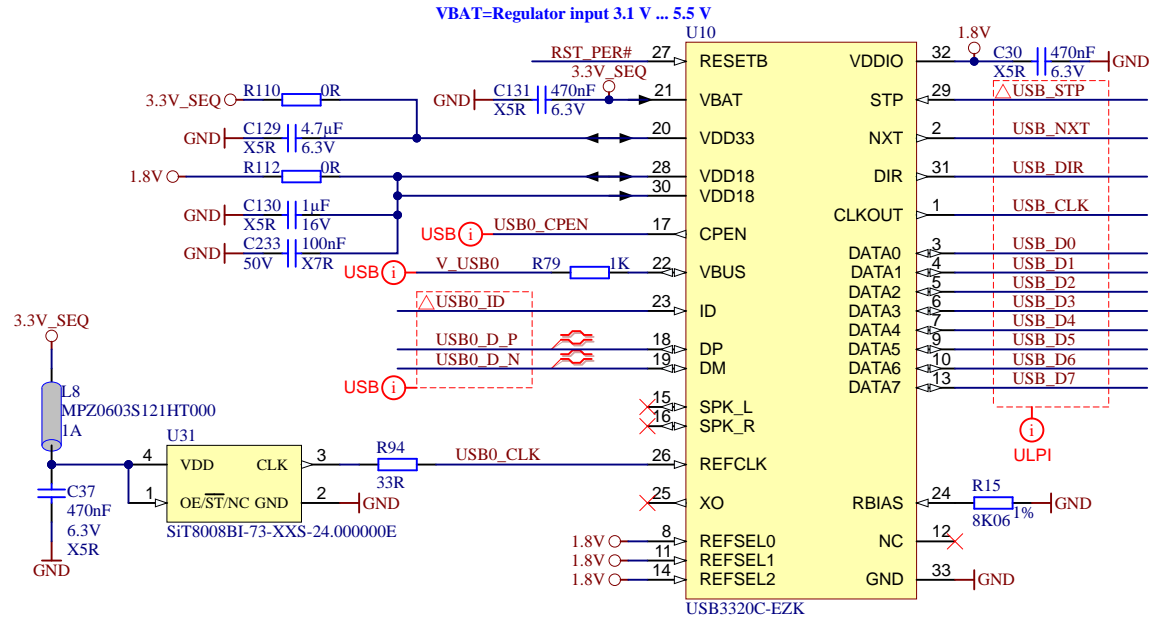




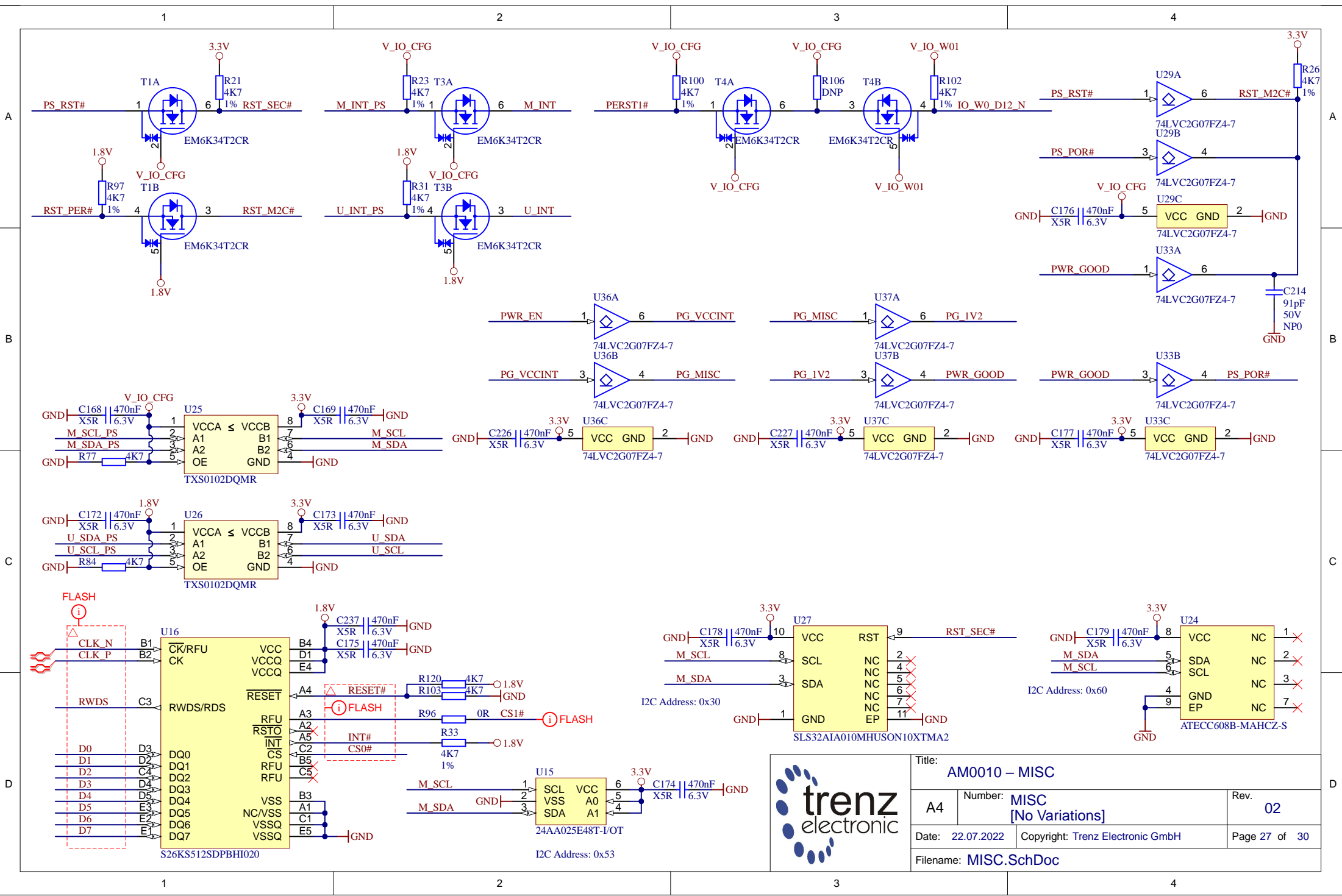
Title: AM0010 – ETHPHY		
A4	Number: ETHPHY [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 25 of 30
Filename: ETHPHY.SchDoc		

## Modify variants!

	USB3320	USB3340
R110	0R	DNP
R112	0R	DNP
C129	4.7 $\mu$ F	1 $\mu$ F
C233	0.1 $\mu$ F	1 $\mu$ F

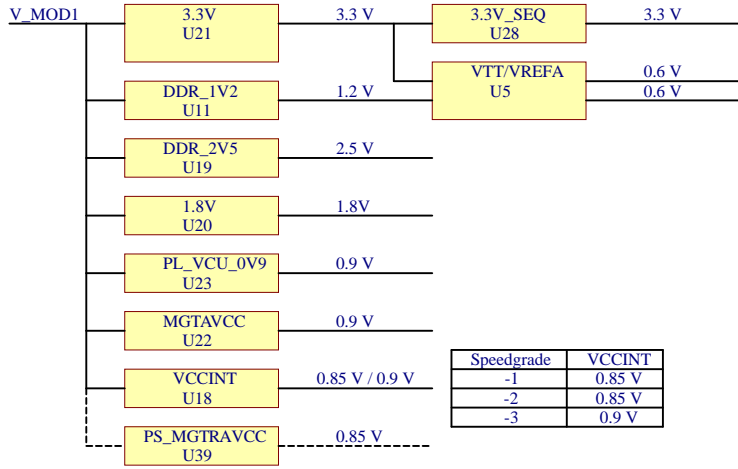


	Title: AM0010 – USBPHY	
	A4	Number: USBPHY [No Variations]
	Date: 22.07.2022	Copyright: Trenz Electronic GmbH
	Filename: USBPHY.SchDoc	
	Rev. 02	Page 26 of 30



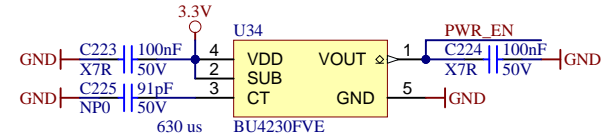
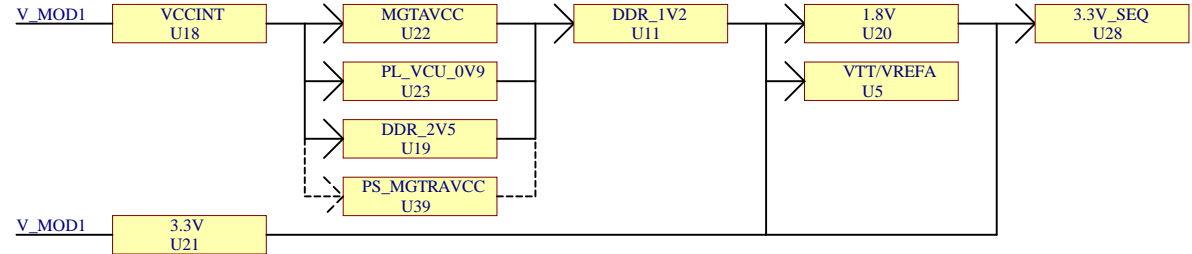
Title: AM0010 – MISC		
A4	Number: MISC [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 27 of 30
Filename: MISC.SchDoc		

### Power Supply Structure



Speedgrade	VCCINT
-1	0.85 V
-2	0.85 V
-3	0.9 V

### Power Supply Sequencing



A

A

B

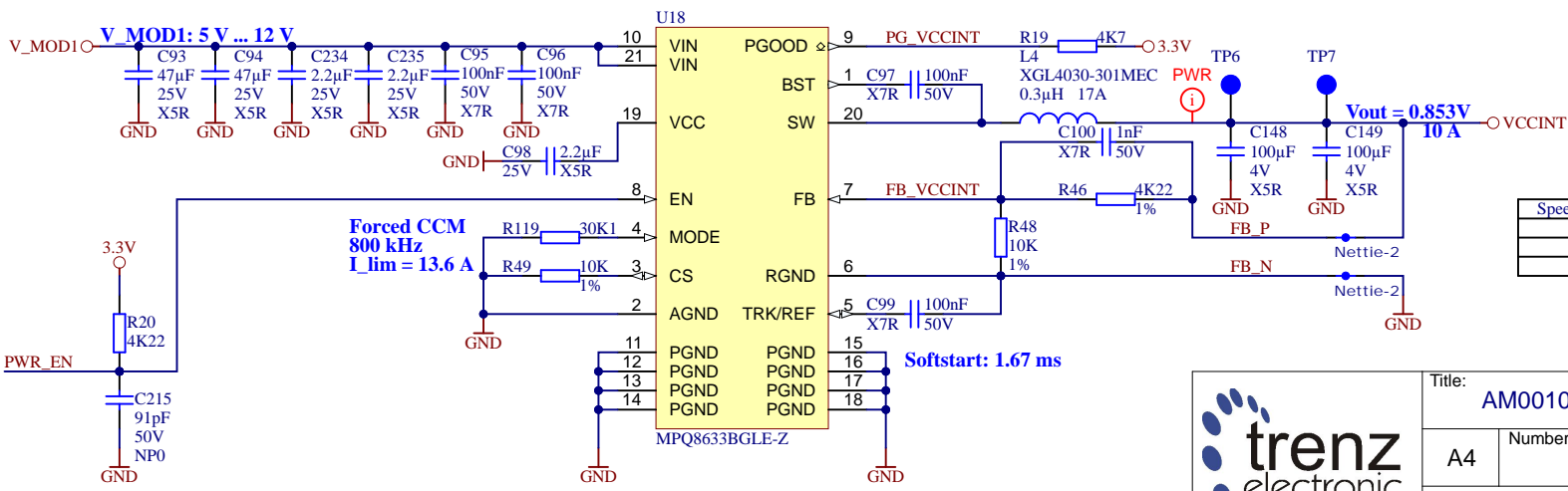
B

C

C

D

D



Speedgrade	R46	R48	C100	VCCINT
-1	4K22	10K	1 nF	0.853 V
-2	4K22	10K	1 nF	0.853 V
-3	10K	20K	680 pF	0.900 V



Title: AM0010 – POWER_1		
A4	Number: POWER_1 [No Variations]	Rev. 02
Date: 02.09.2022	Copyright: Trenz Electronic GmbH	Page 28 of 30
Filename: POWER_1.SchDoc		

A

A

B

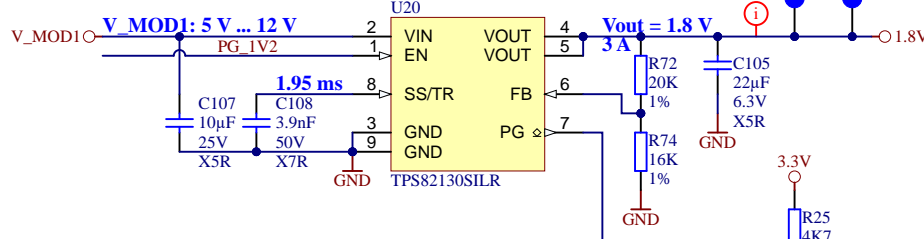
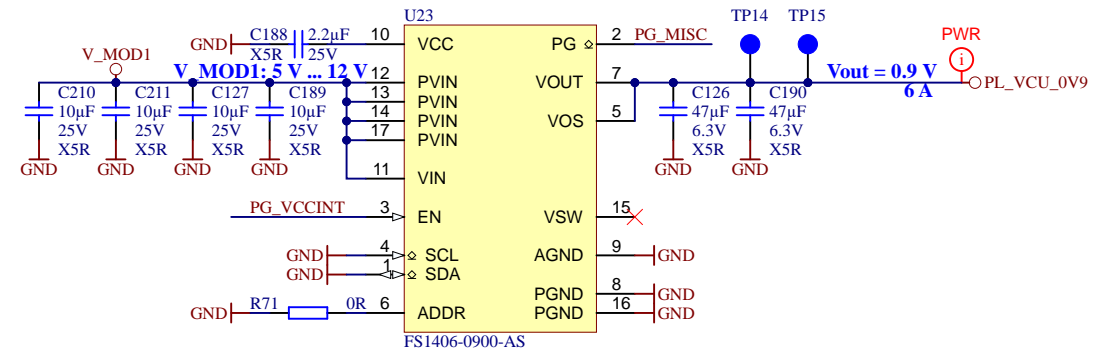
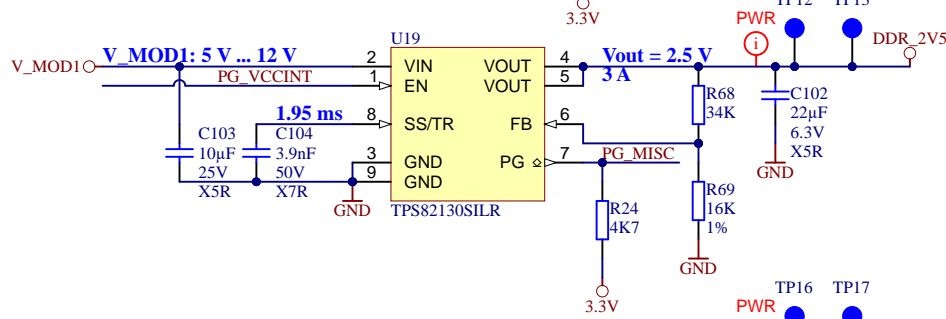
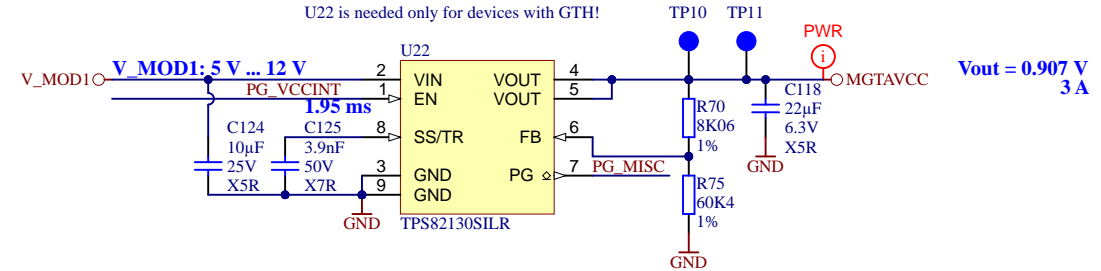
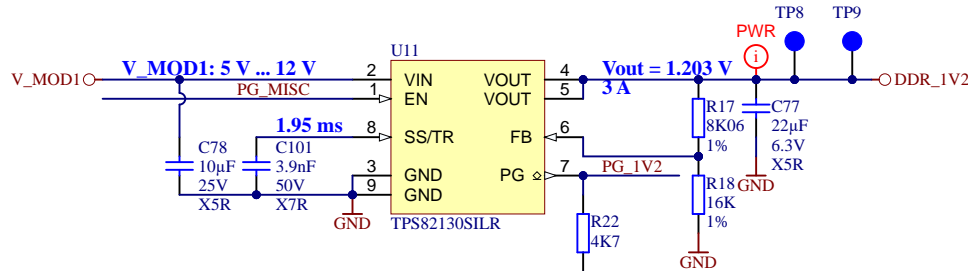
B

C

C

D

D



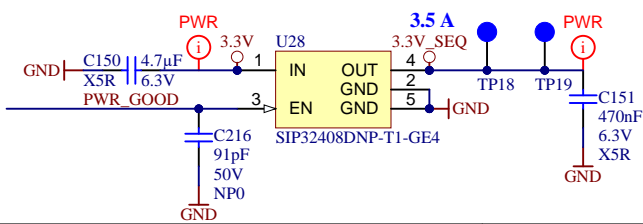
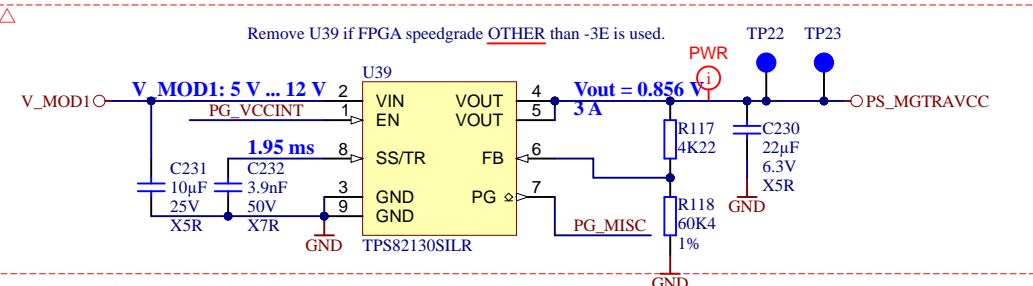
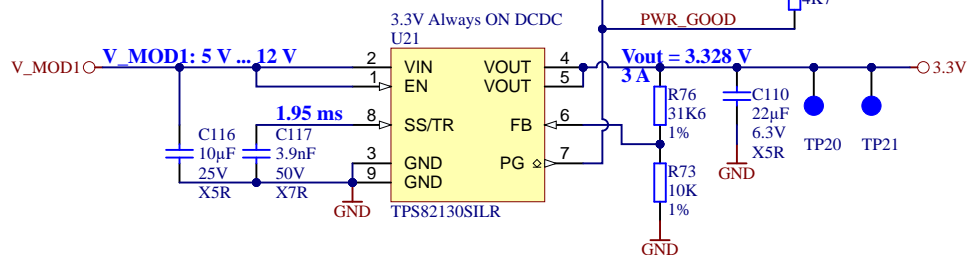
Modify variants!

Speedgrade	L14	VCCINT
-1	L14	0.85 V
-2	L14	0.85 V
-3	DNP	0.9 V

Remove L14 when FPGA speedgrade -3E is used

VCCINT - L14 (3A) - PS\_MGTRAVCC (120 Ohm@100 MHz)

Vout\_max = 0.876V (+3%)  
Vout\_nom = 0.85V  
Vout\_min = 0.833V (-2%)



Title: AM0010 - POWER_2		
A4	Number: POWER_2 [No Variations]	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 29 of 30
Filename: POWER_2.SchDoc		

